

# COMPAL CONFIDENTIAL

MODEL NAME :DDA30

PCB NO : LA-F292P

BOM P/N :

Port Map:

Kirkwood MLK Port Map as of 2017-04-13

## X9 KBL UMA U42

**Kabylake R**

**2017-11-14**

**REV : 1.0(A00)**

@ : Nopop Component  
EMI@ : EMI Component  
@EMI@ : EMI Nopop Component  
ESD@ : ESDComponent  
@ESD@ : ESD Nopop Component  
RF@ : RF Component  
@RF@ : RF Nopop Component  
CXDP@ : XDP Component  
CONN@ : Connector Component  
ESPI@ : ESPI interface Component  
LPC@ : External ESPI Component (SHD)  
U42@ : KBL-R U42 Component  
U22@ : KBL-R U22 Component  
DS3@ : Support DS3 Component  
NDS3@ : No Support DS3 Component

RTD3@ : Support RTD3 Component  
NRTD3@ : No Support RTD3 Component  
@RTD3@ : Reserve RTD3 Component

MB PCB

Part Number	Description
DAB00025010	PCB 26B LA-F292P REV1 MB UMA AR 2

Layout Dell logo



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REV:X00  
PWB:

PWR CKT:0810

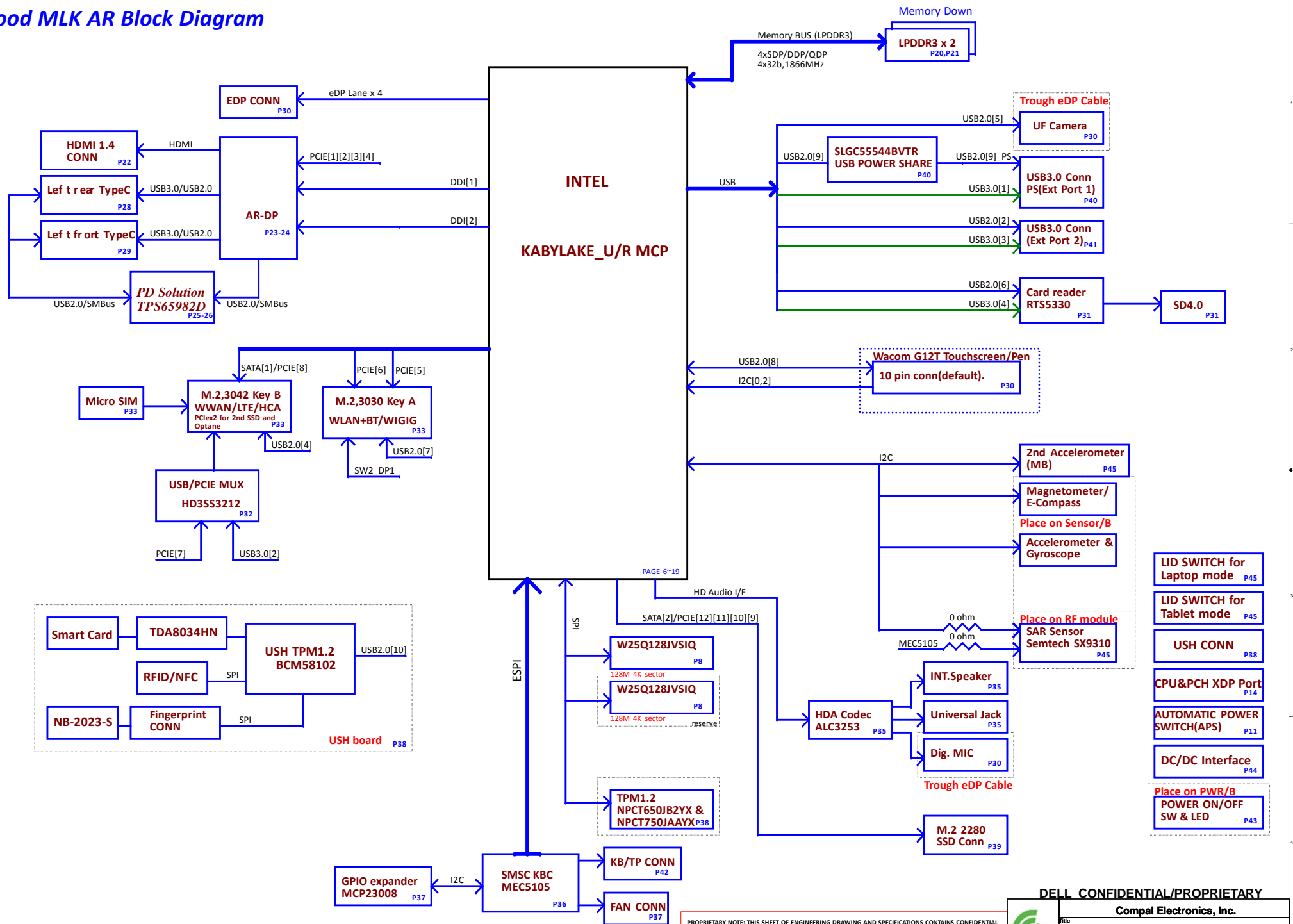
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# Kirkwood MLK AR Block Diagram



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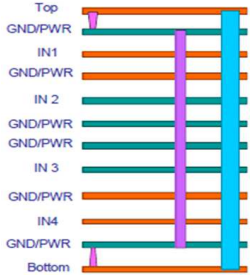
POWER STATES

Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
State									
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State	power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN	+3.3V_M	(M-OFF) +3.3V_M +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA
S0		ON	ON	ON	ON	ON
S3		ON	ON	OFF	ON	OFF
S5 S4/AC		ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist		OFF	OFF	OFF	OFF	OFF

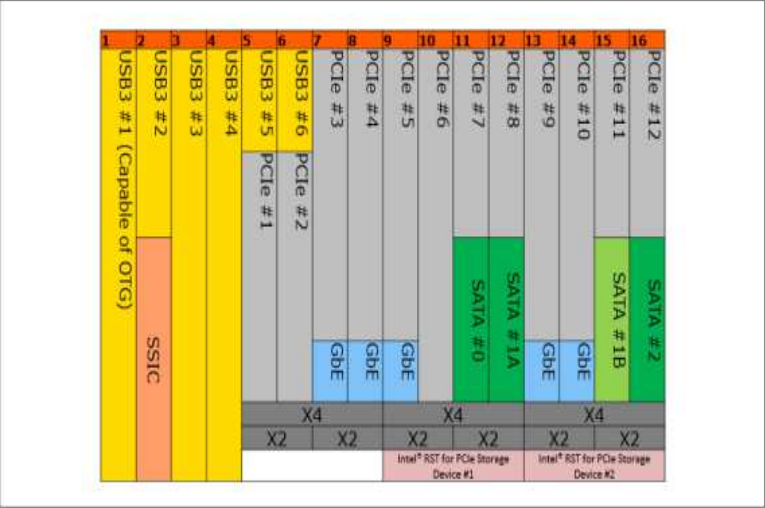
Layer NO.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			Solder Mask	DS7402	0.50
1	Top(GND)		copper foil+plating	0.33oz+plating	1.40
		3.73	Prepreg	106	0.00
2	VCC/GND		copper foil+plating	0.33oz+plating	1.20
		3.77	Prepreg	106	0.00
3	IN1		copper foil	0.50oz	0.65
		4	CORE	3mil	1.00
4	VCC/GND		copper foil	0.50oz	0.65
		3.91	Prepreg	1080	0.65
5	IN1		copper foil	0.50oz	0.65
		4	CORE	3mil	1.00
6	VCC/GND		copper foil	0.50oz	0.65
		3.91	Prepreg	1080	0.65
7	VCC/GND		copper foil	0.50oz	0.65
		4	CORE	3mil	1.00
8	IN1		copper foil	0.50oz	0.65
		3.91	Prepreg	1080	0.65
9	VCC/GND		copper foil	0.50oz	0.65
		4	CORE	3mil	1.00
10	IN1		copper foil	0.50oz	0.65
		3.77	Prepreg	106	0.00
11	VCC/GND		copper foil+plating	0.33oz+plating	1.20
		3.71	Prepreg	106	0.00
12	Bottom(GND)		copper foil+plating	0.33oz+plating	1.40
			Solder Mask		0.50
Over all Thickness(1.0MM ± 0.05)				39.37	39.35



USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Left
USB3.0-4				SD Card Reader
USB3.0-5		PCIE-1		Alpine Ridge-DP
USB3.0-6		PCIE-2		
		PCIE-3		
		PCIE-4		
		PCIE-5		M.2 3030(WLAN)
		PCIE-6		M.2 3030(WIGIG)
		PCIE-7	SATA-0	M.2 3042(SATA Cache or HCA)
		PCIE-8	SATA-1	
		PCIE-9		M.2 2280 SSD (PCIe4 or SATA)
		PCIE-10		
		PCIE-11	SATA-1*	
		PCIE-12	SATA-2	

USB PORT#	DESTINATION
1	TYPEC Front Side
2	JUSB2-->Left
3	TYPEC Rear Side
4	M2 3042(WWAN)
5	UF Camera
6	SD Card Reader
7	M.2 3030(BT)
8	Touch Screen
9	JUSB1-->Right
10	USH

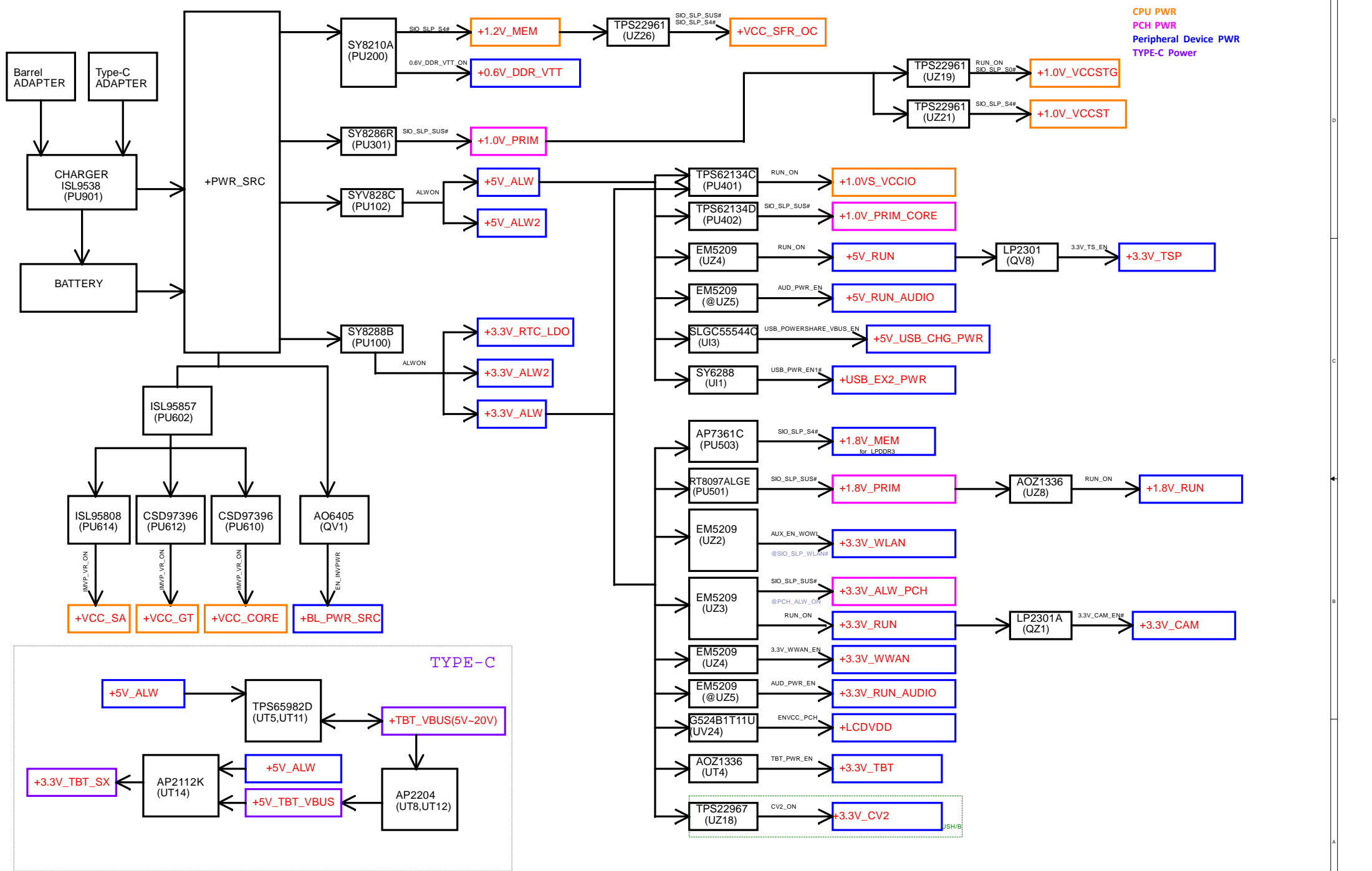
High Speed I/O (HSIO) Lane Multiplexing in KBL U



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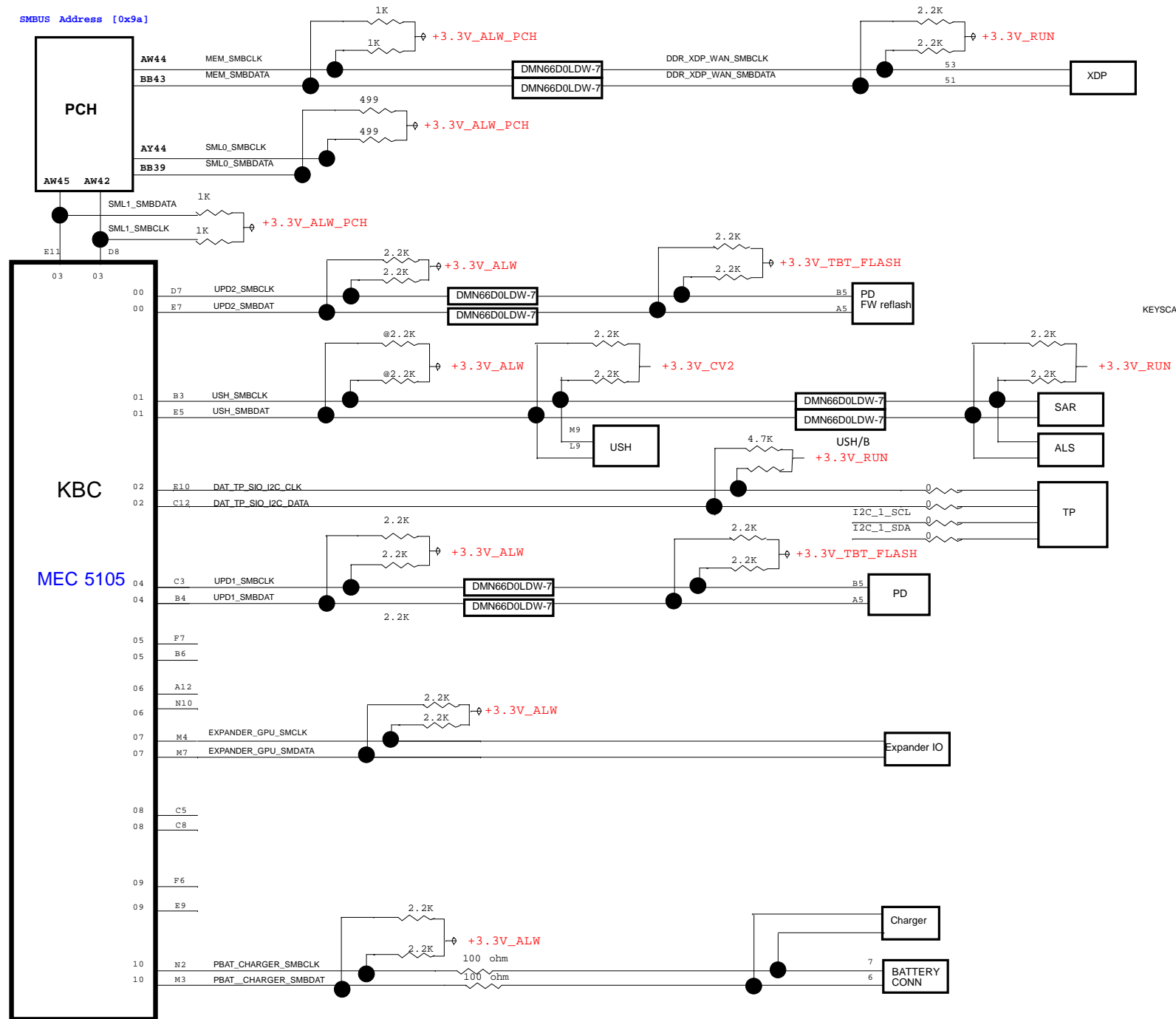
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CPU PWR  
PCH PWR  
Peripheral Device PWR  
TYPE-C Power

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SMBUS Address [0x9a]



MEC 5105

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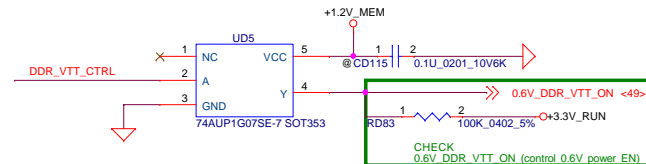
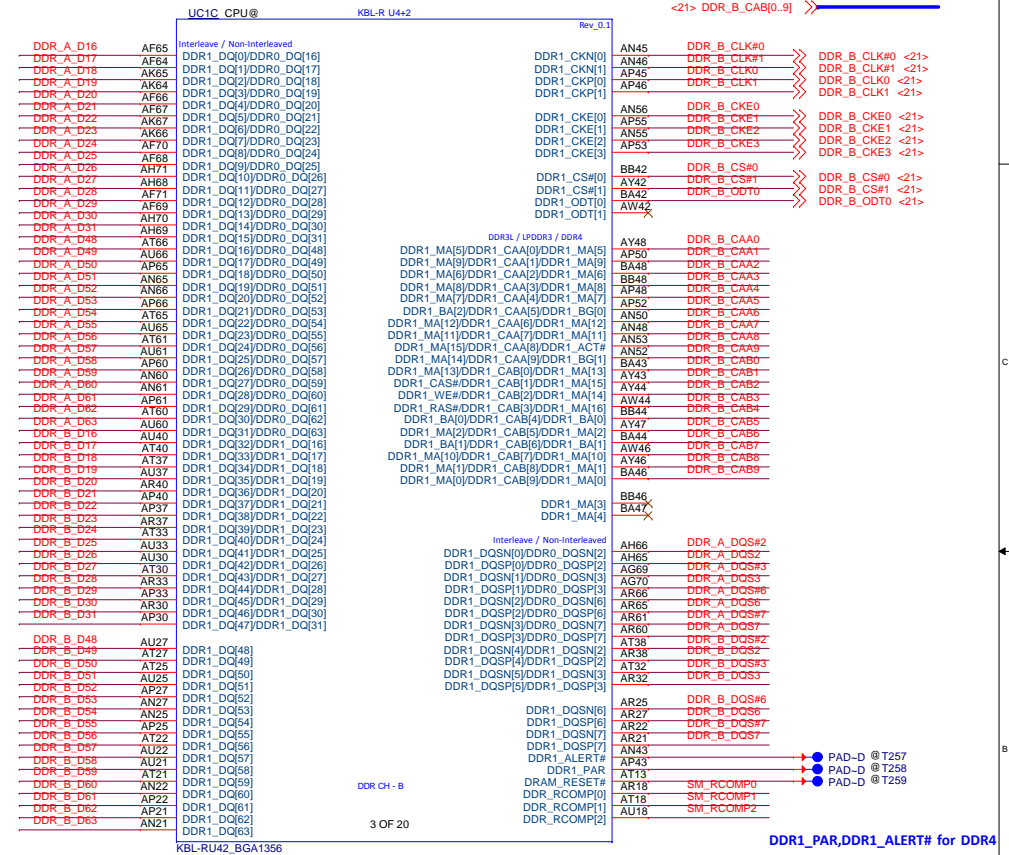
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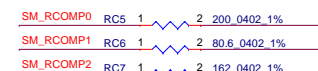




### LPDDR3, Ballout for side by side(Non-Interleave)



## LPDDR3 COMPENSATION SIGNALS



CAD Note:  
Trace width=12~15 mil, Spacing=20 mils  
Max trace length= 500 mil

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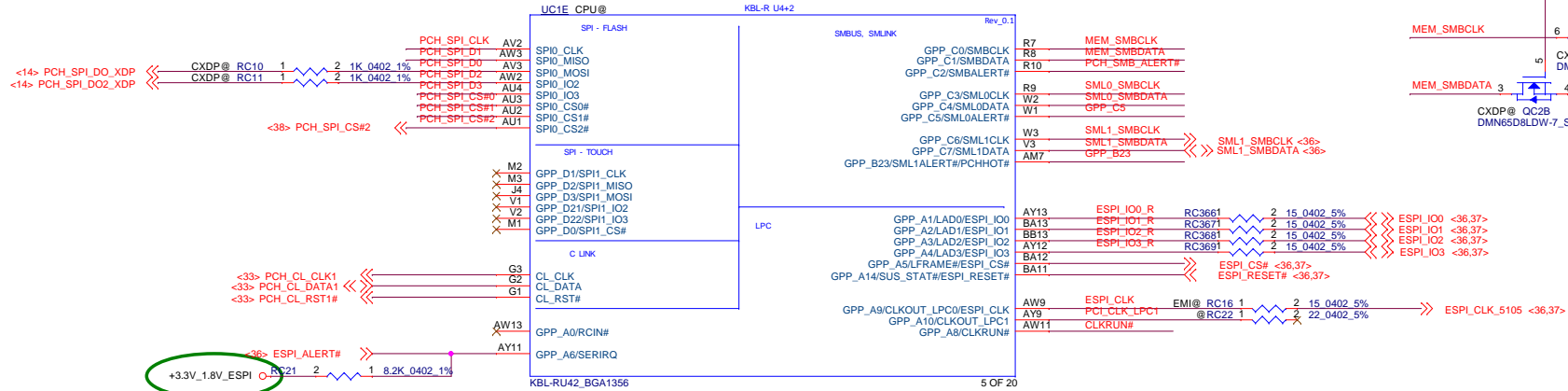
CPU (2/14)

**LA-F292P**

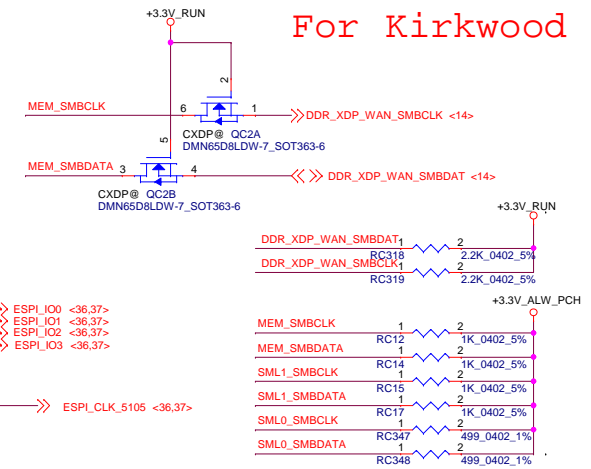
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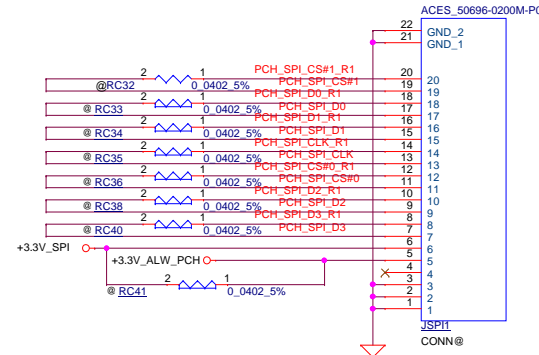
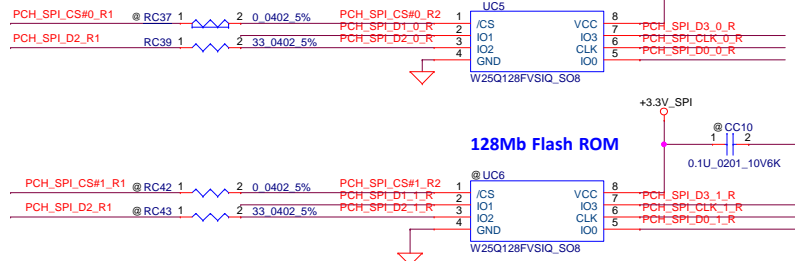
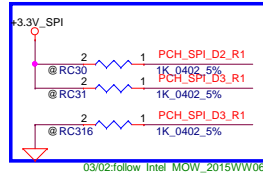
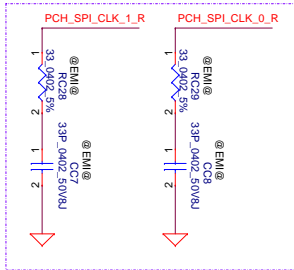
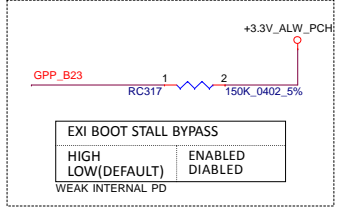
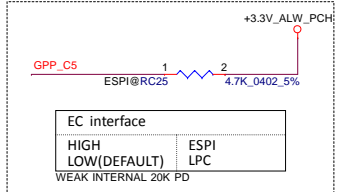
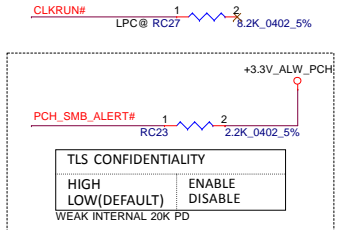
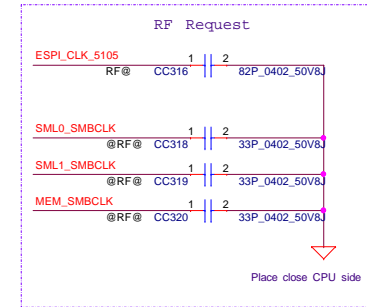
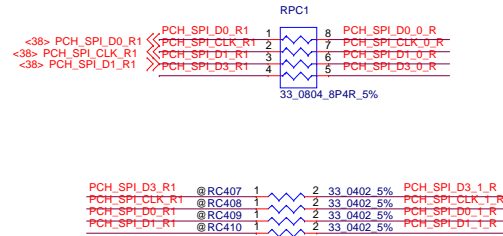
SPI\_MOSI= SPI\_IO0  
SPI\_MISO= SPI\_IO1  
PCH EDS R0.7 p.235~236



For Kirkwood



#### SOFTWARE TAA



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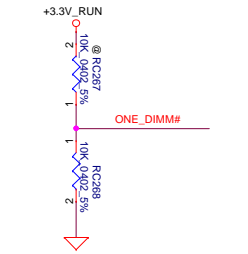
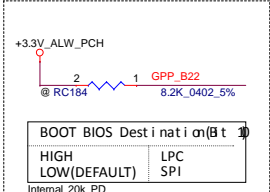
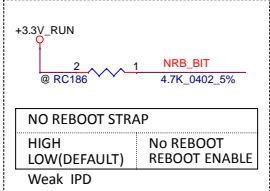
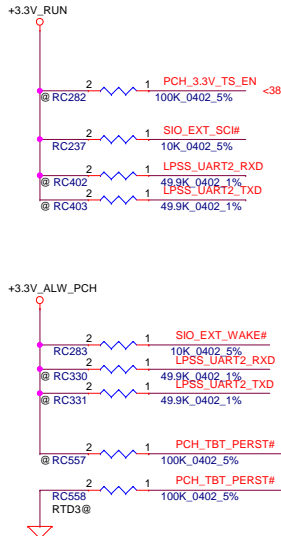
CPU (3/14)

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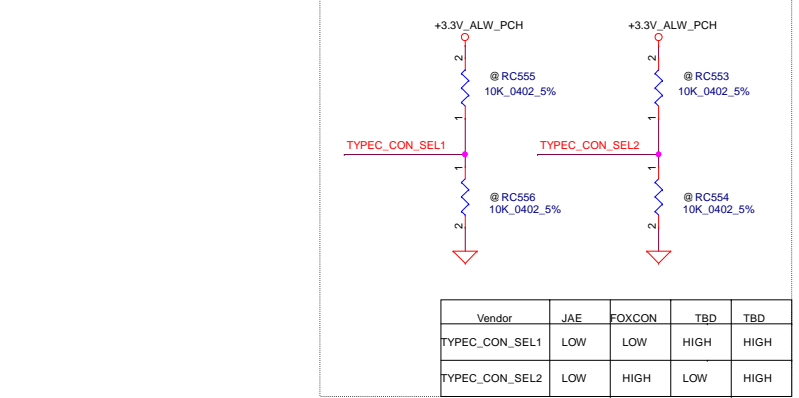
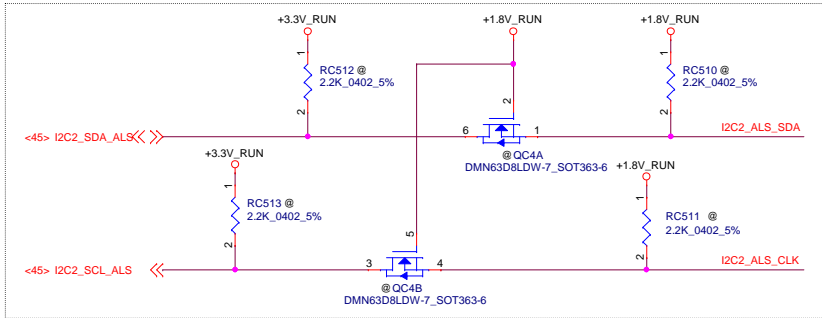
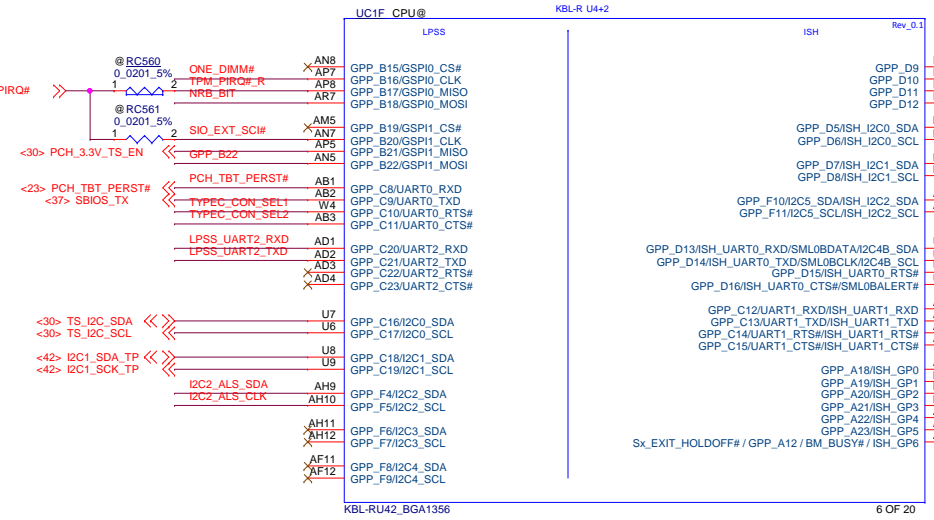
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Size	Document Number		Rev
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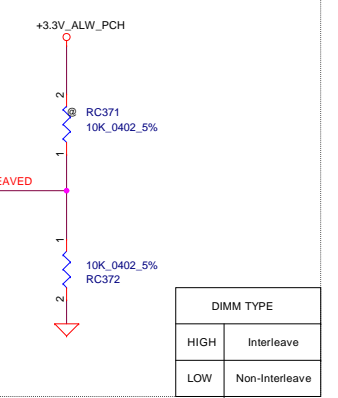
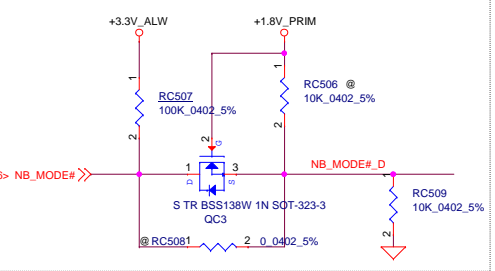
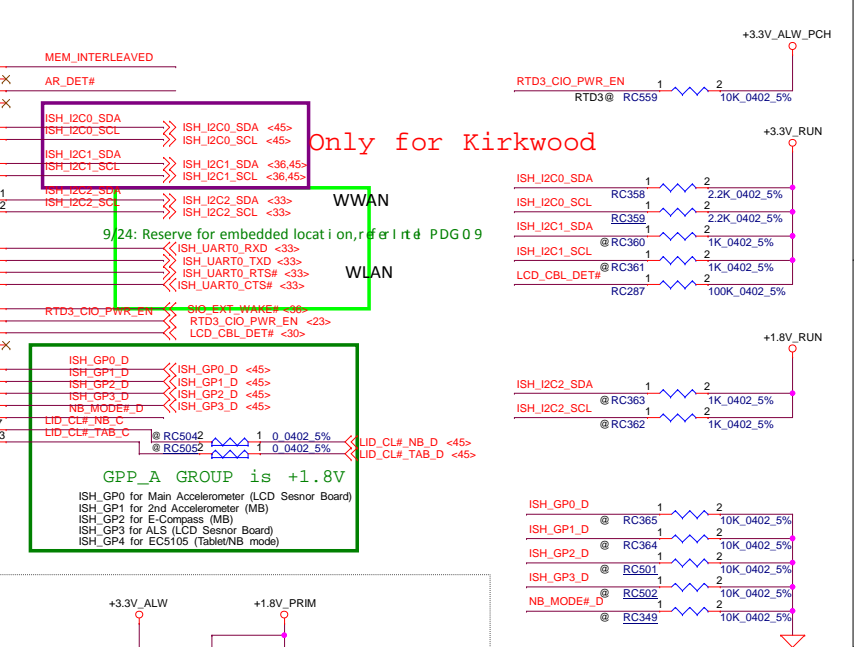




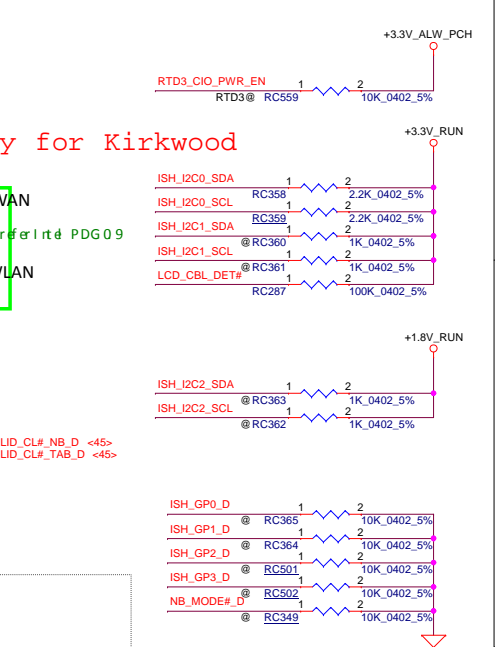
DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM



Vendor	JAE	FOXCON	TBD	TBD
TYPECON_SEL1	LOW	LOW	HIGH	HIGH
TYPECON_SEL2	LOW	HIGH	LOW	HIGH



DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave

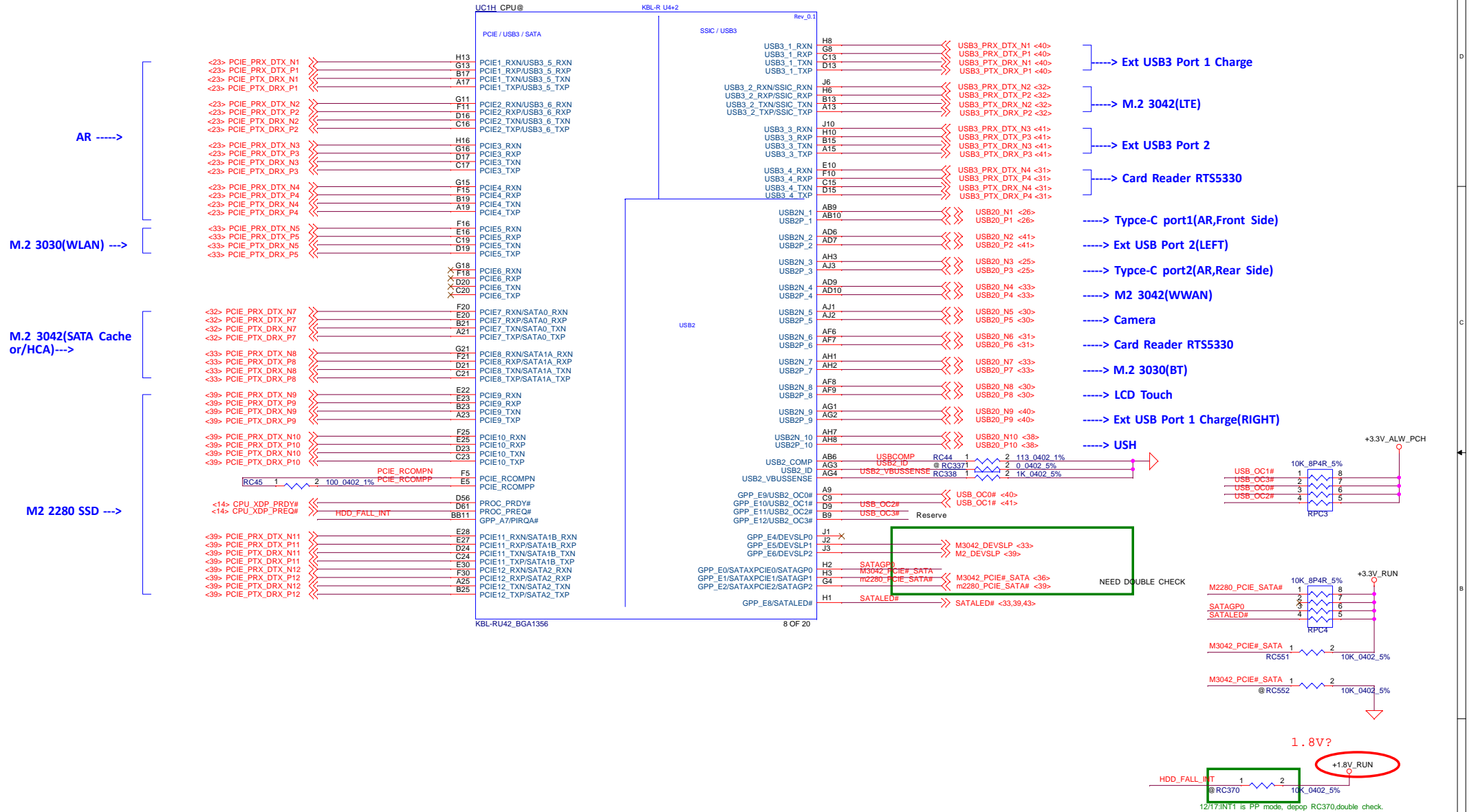


AR_DET#	
HIGH	NON AR
LOW	AR

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# For AR, Kirkwood



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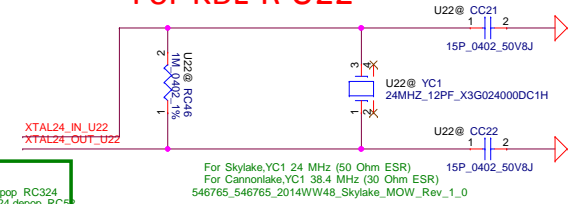
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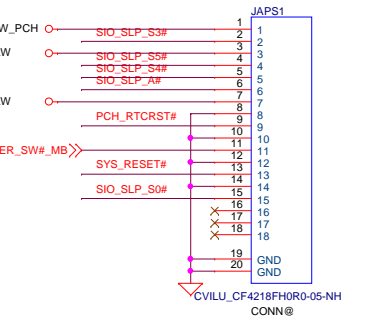
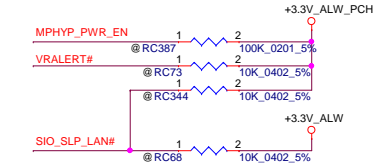
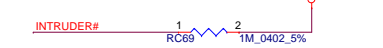
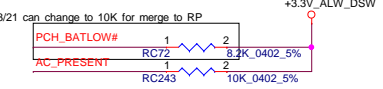
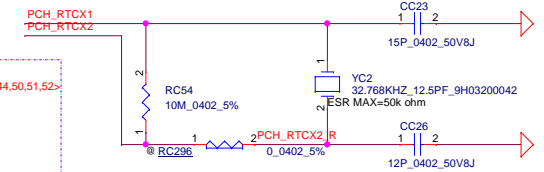
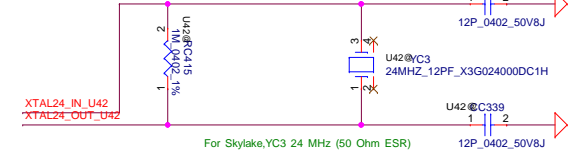
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# For UMA CONFIG For KBL-R U22

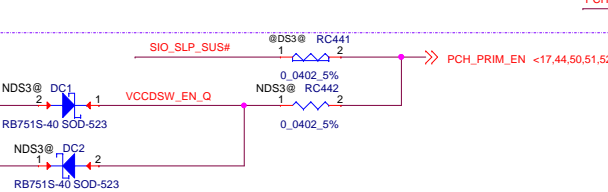
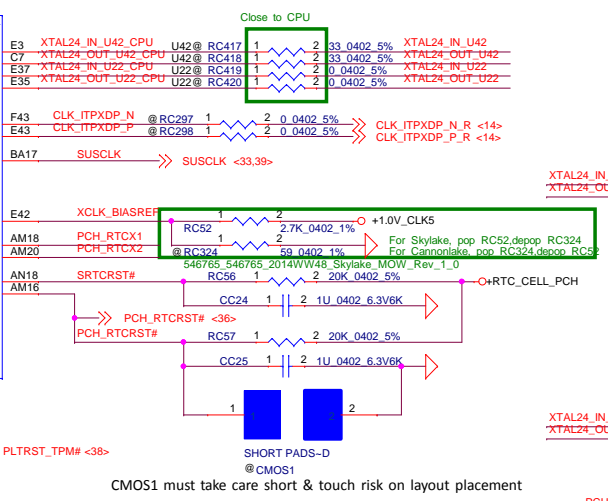
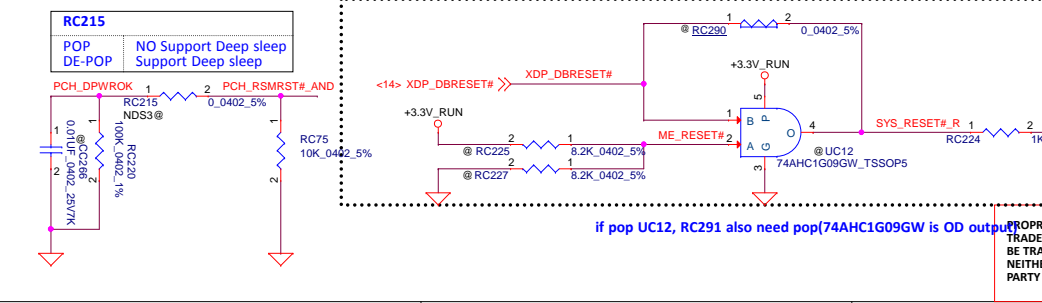
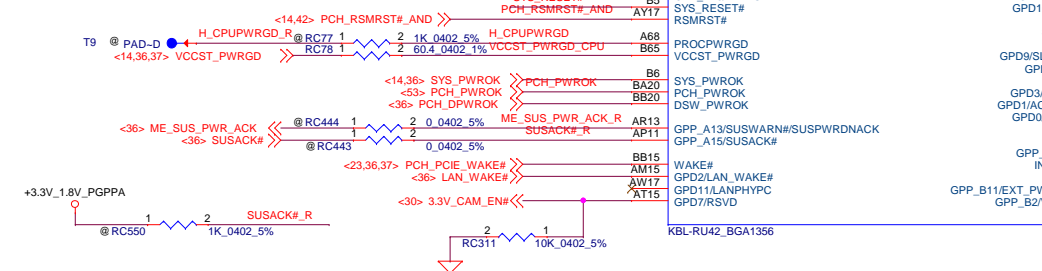
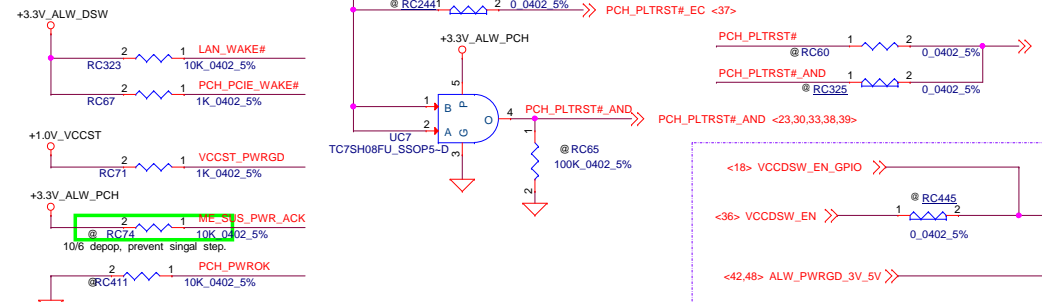
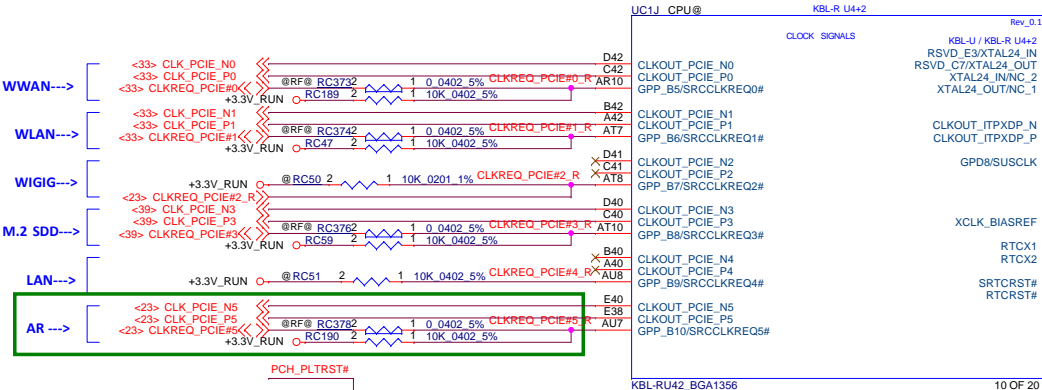


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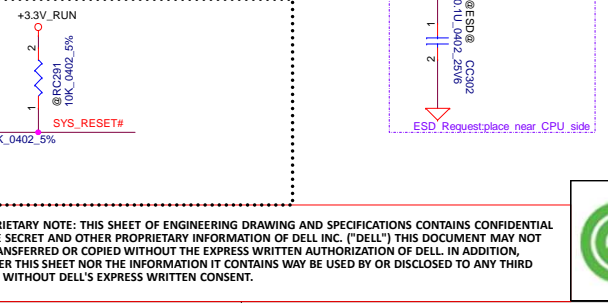
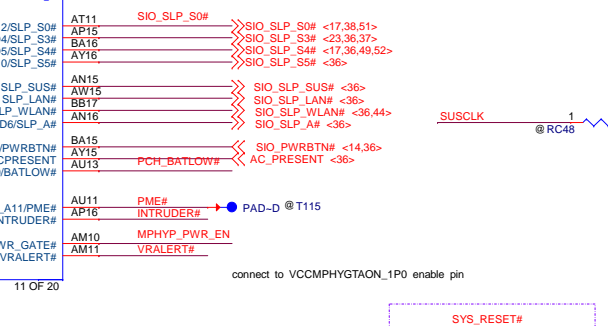
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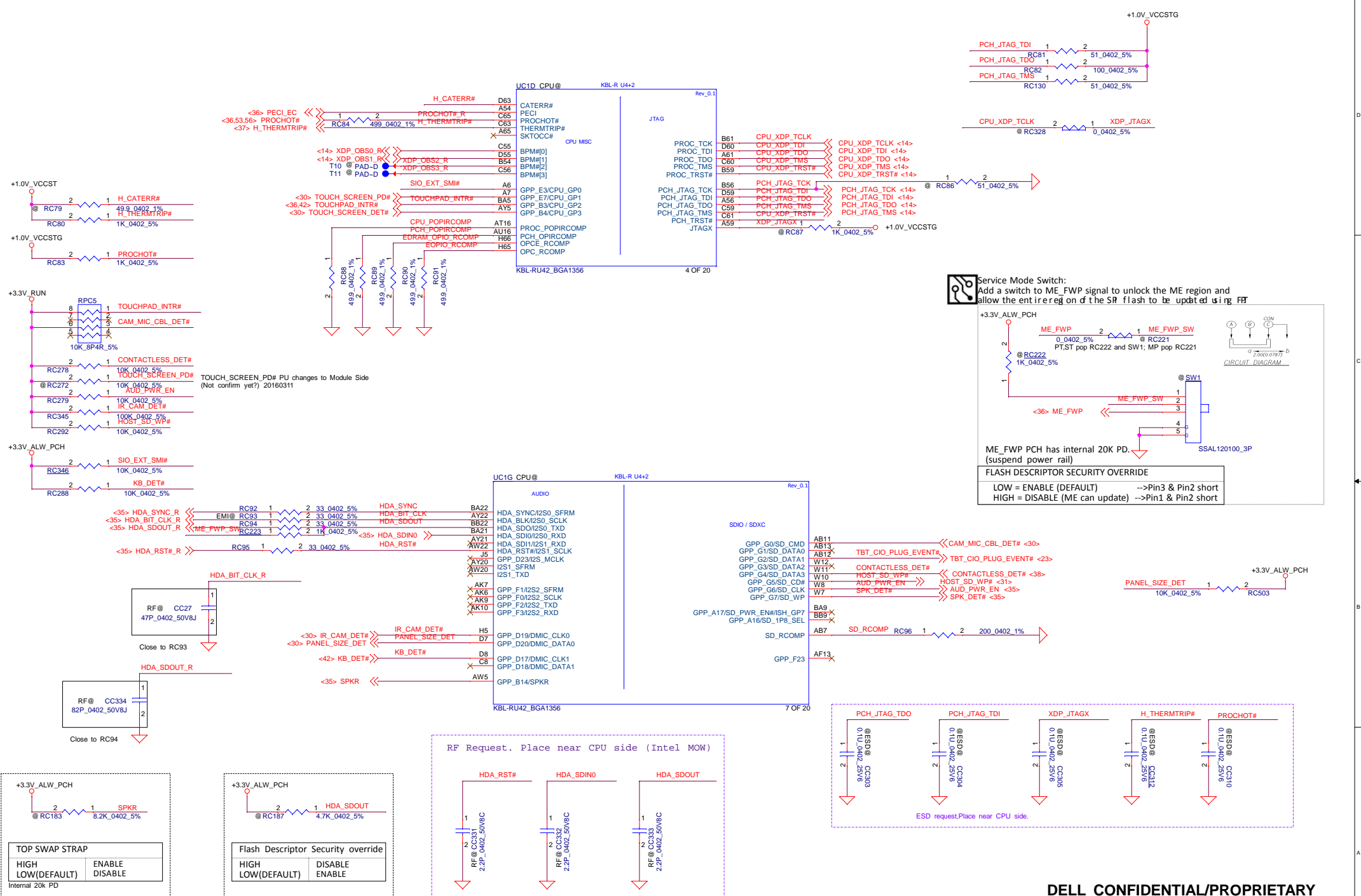


	RC439	RC440	RC536	RC215	RC441	RC442
Support DS3	V	X	V	X	V	X
No Support DS3	X	V	X	V	X	V

'V' mean POP, 'X' mean DE-POP



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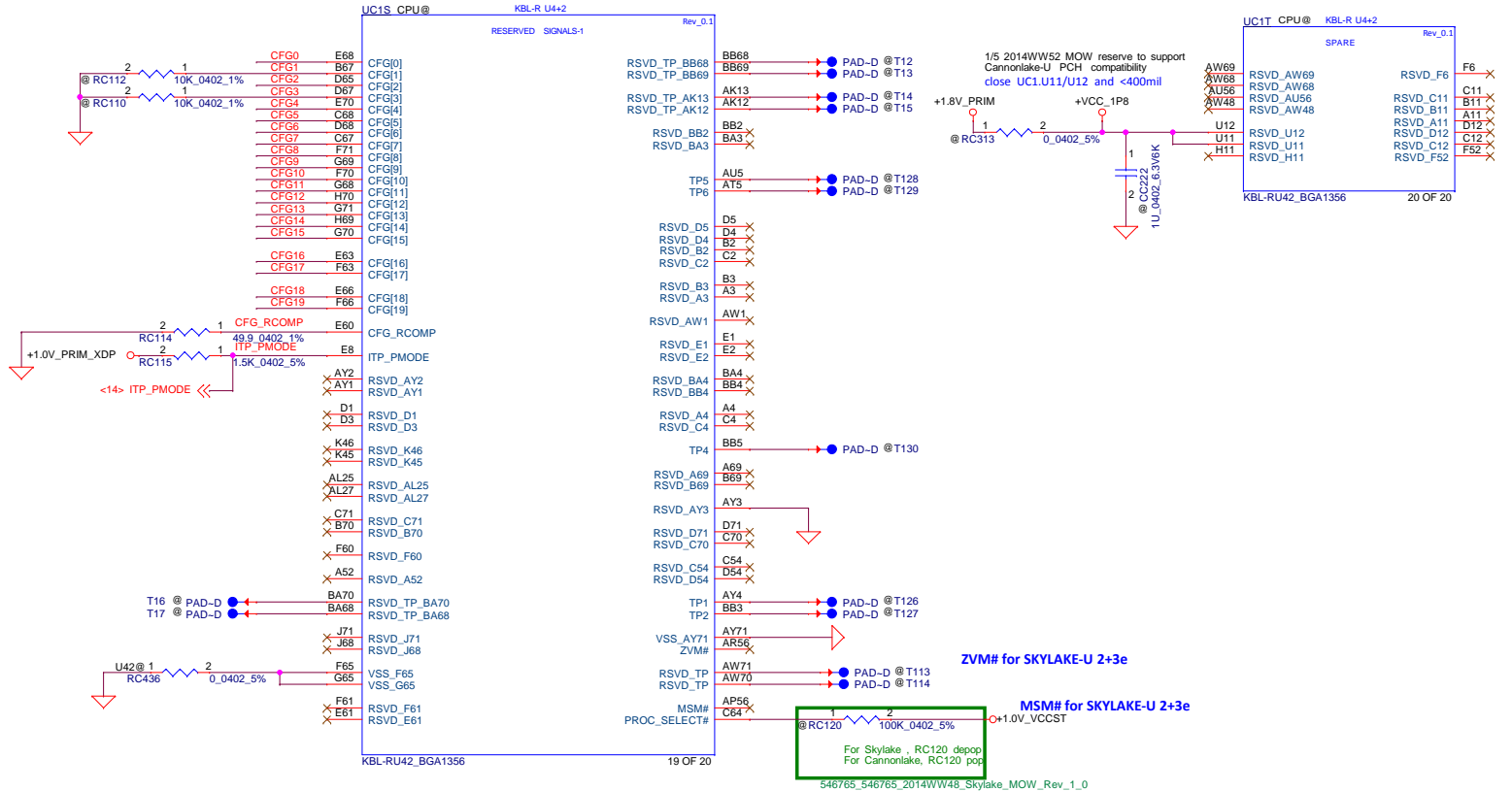
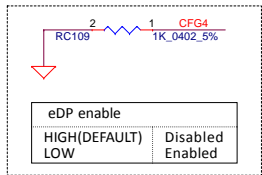
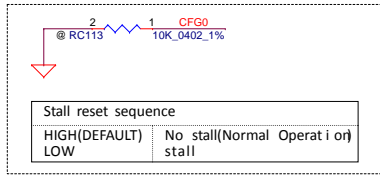
CPU (7/14)

LA-F292P

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Date	Tuesday, November 14, 2017	Sheet 12 of 60

<14> CFG0[0..19] <<

### CFG[2][5][6][7] for SKYLAKE-H CPU CFG strap pin



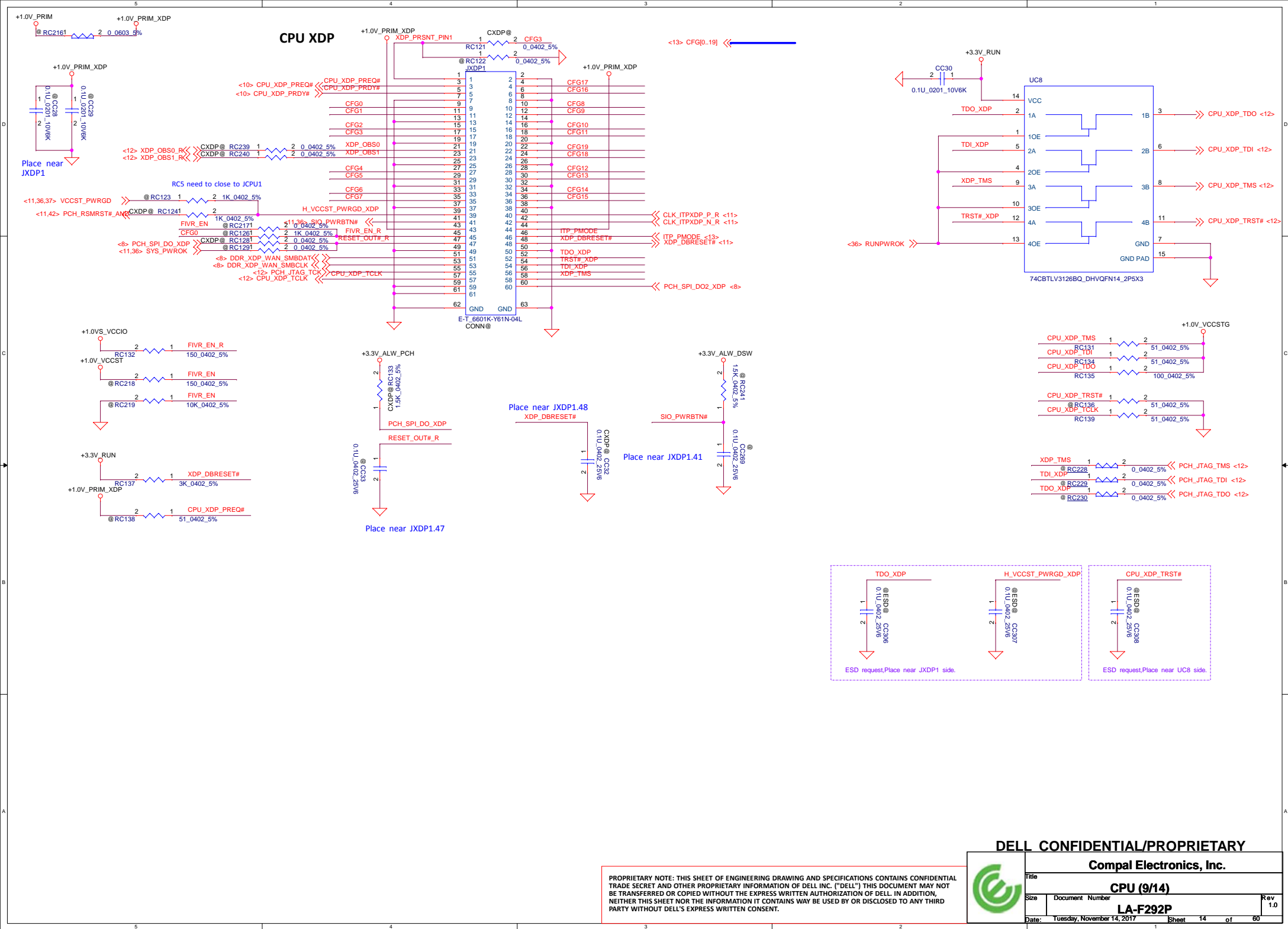
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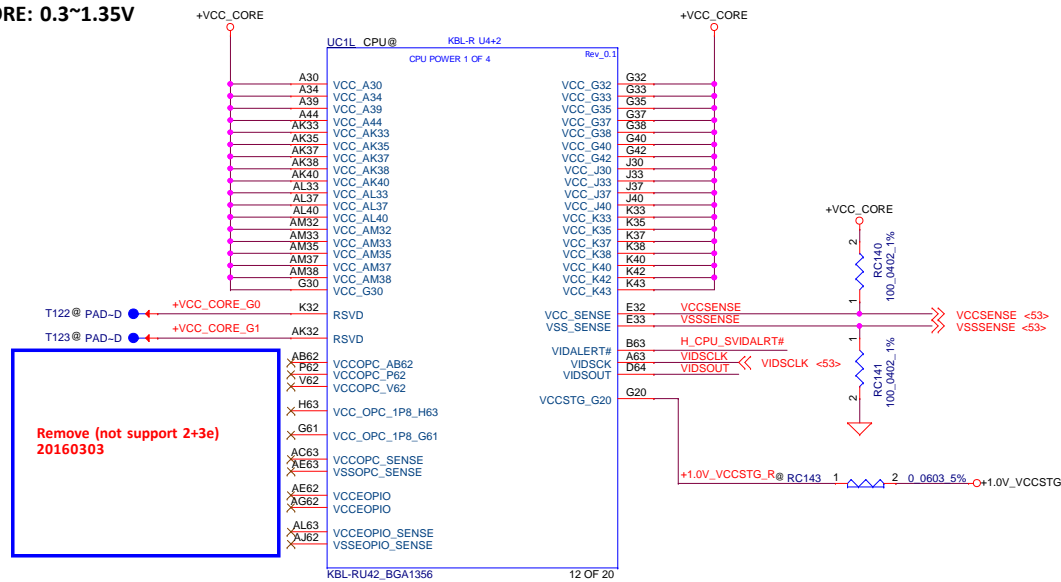
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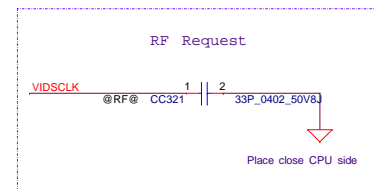
+VCC\_CORE: 0.3~1.35V



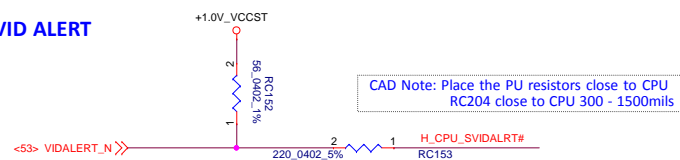
VCCOPC,VCCOPC\_1P8,VCCEPIO for SKYLAKE-U 2+3e  
(w/ on package cache)

PSC(Primary side cap) : Place as close to the package as possible  
BSC(Backside cap) : Place on secondary side, underneath the package

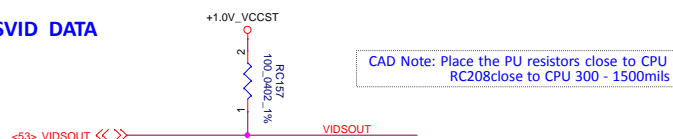
Component placement order:  
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source



## SVID ALERT



## SVID DATA



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KBL-R 4+2 and KBL-U 2+2&2+3e opt i on( p l a c e o n p o w e r p a g e)



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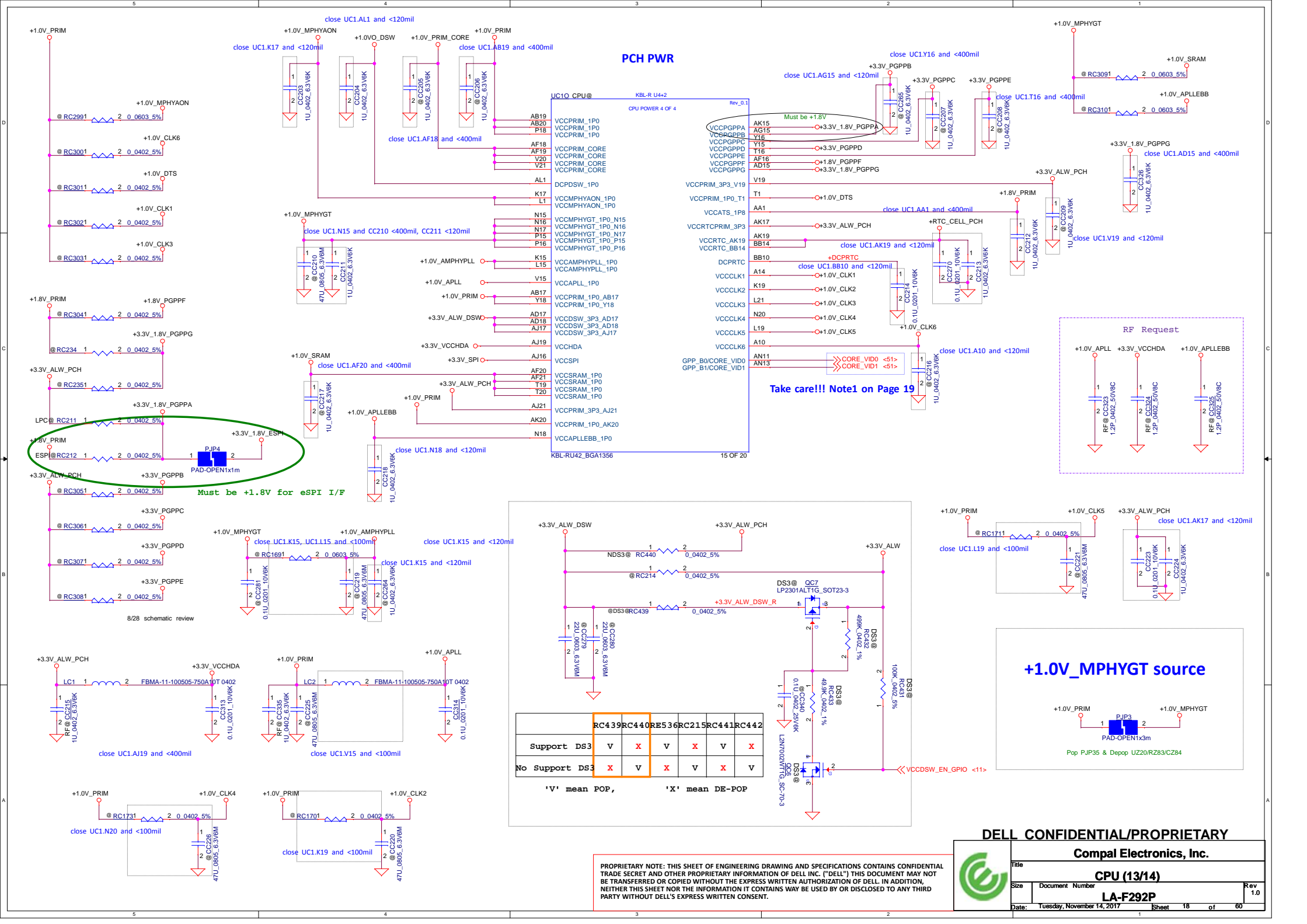
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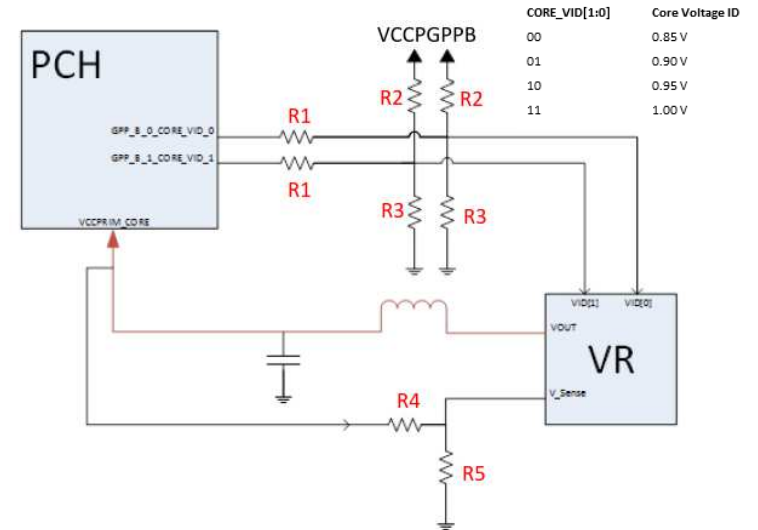
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Note1: VCCPRIM\_CORE Implementat i on w th PCH CORE\_V D Reco mmendati on

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



For Pre-ES Parts: Disconnect PCH CORE\_VID[1:0] to the VR and fix PCH VCCPRIM\_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM\_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE\_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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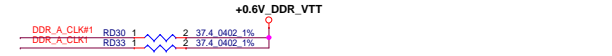
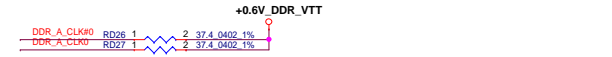
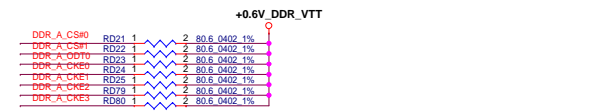
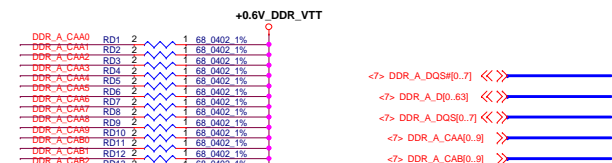
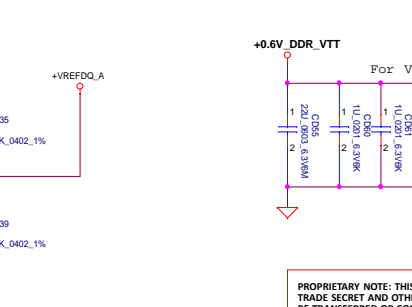
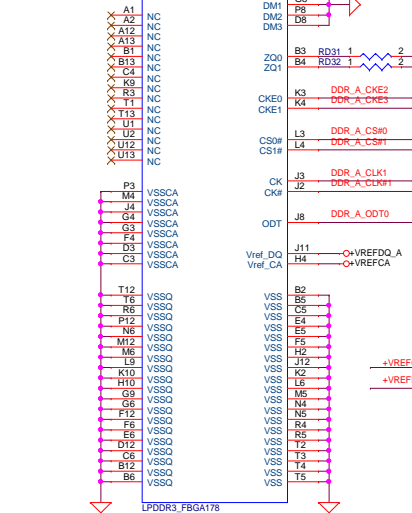
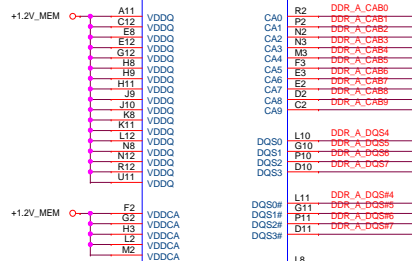
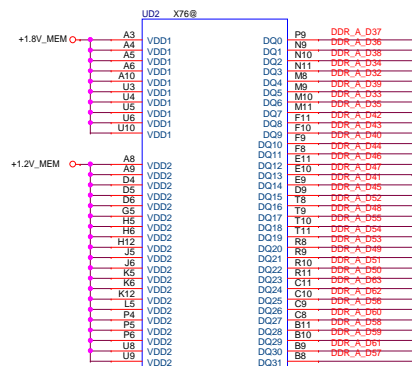
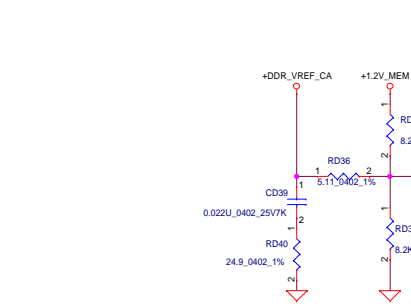
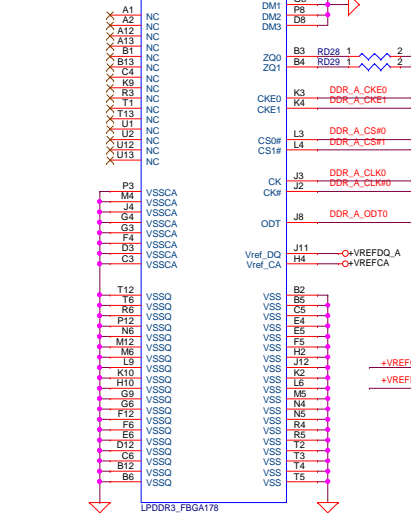
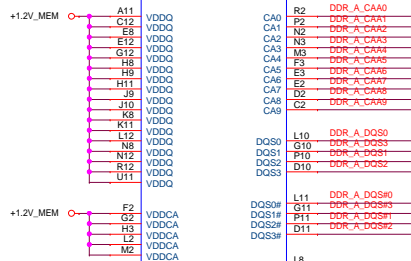
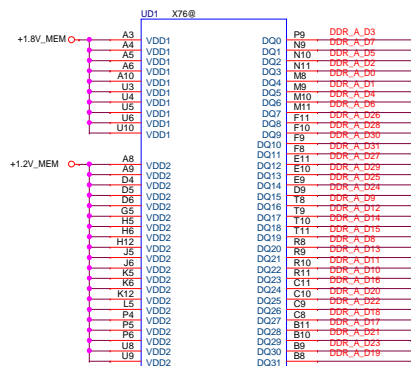
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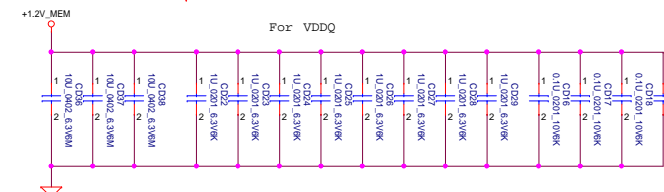
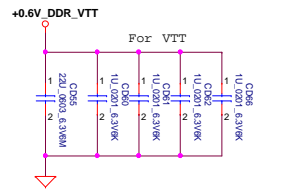
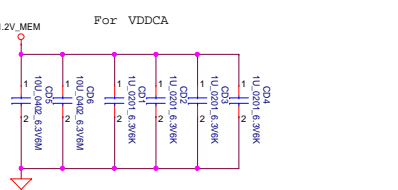
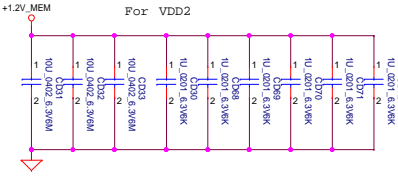
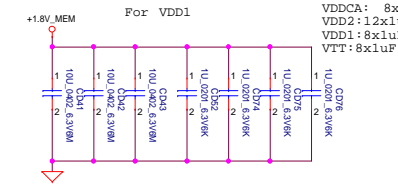
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# For LPDDR3



Follow CRB 544250  
CA - 68 ohm  
CS/CKE/ODT - 80.6 ohm  
CLK - 37.4 ohm

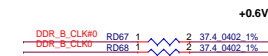
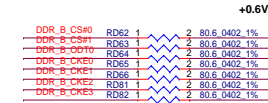
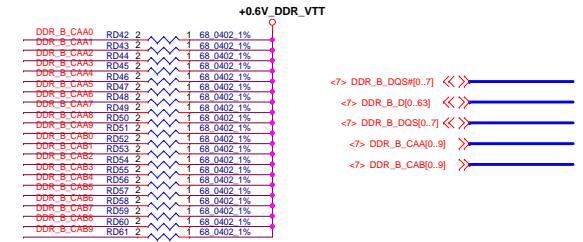
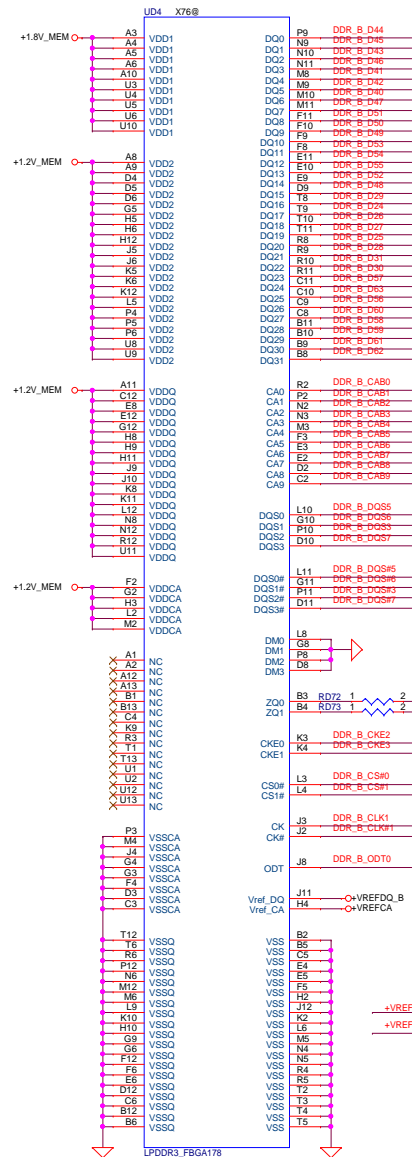
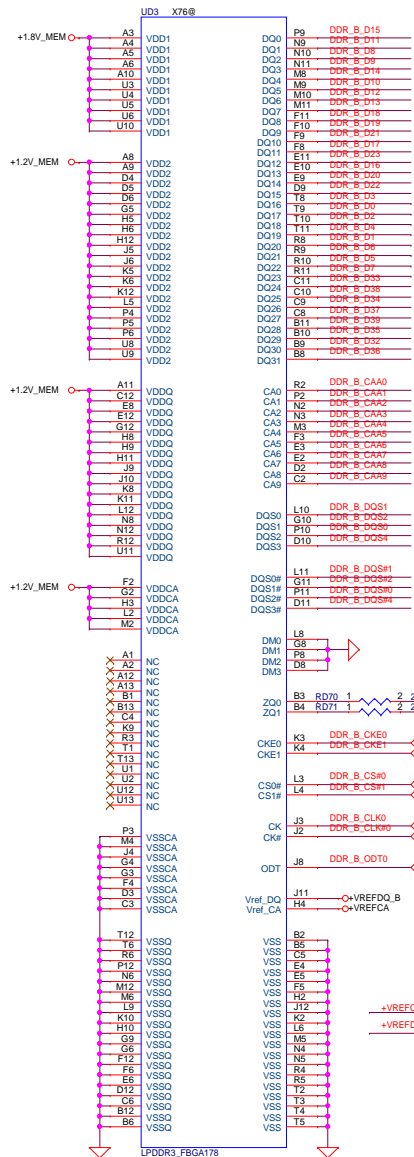
Total  
VDD : 8x0.1uF, 16x1uF, 5x10uF  
VDDCA : 8x1uF, 3x10uF  
VDD2 : 12x1uF, 5x10uF  
VDD1 : 8x1uF, 5x10uF  
VTT : 8x1uF, 2x22uF



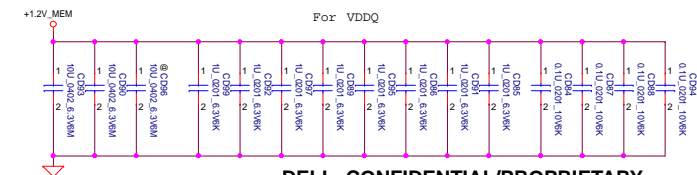
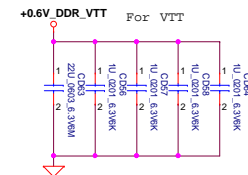
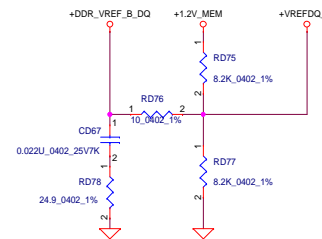
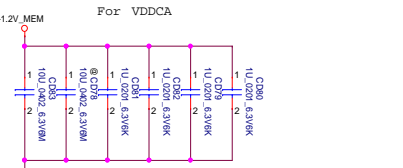
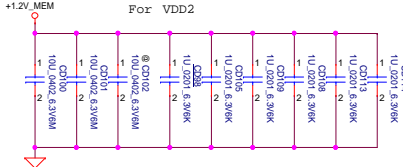
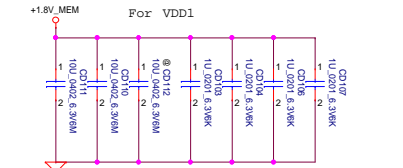
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For LPDDR3

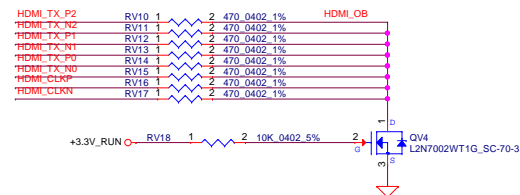
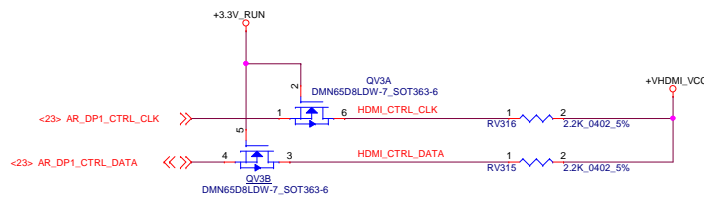
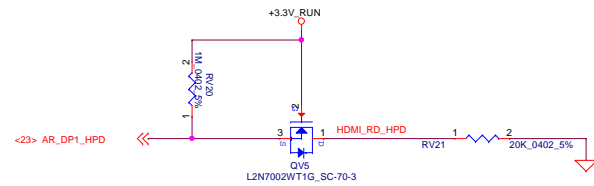
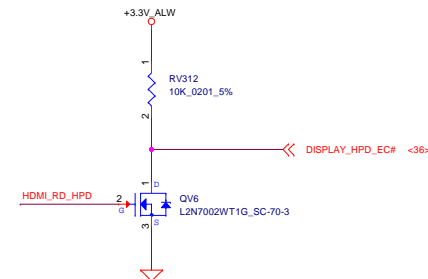
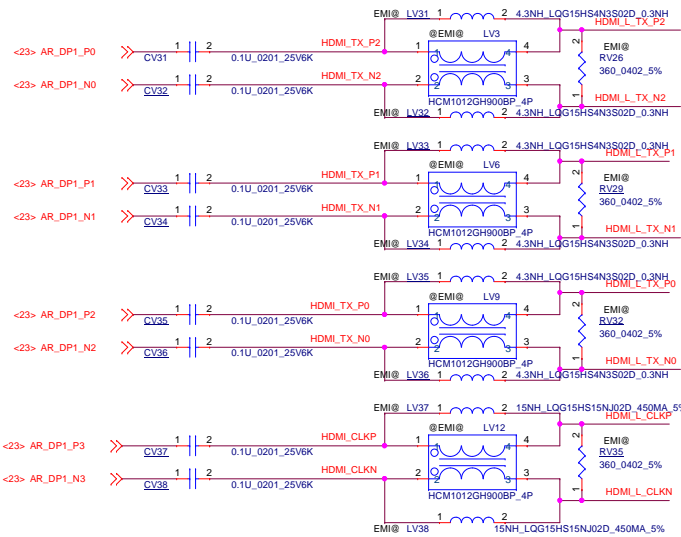
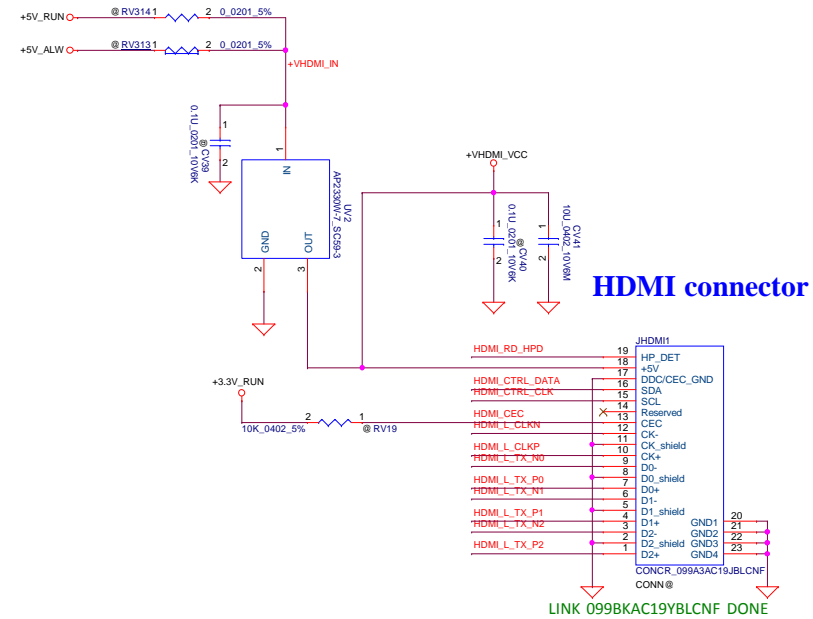


Follow CRB 544250  
CA - 68 ohm  
CS/CKE/ODT - 80.6 ohm  
CLK - 37.4 ohm



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For passive level shifter from PS8339



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HDMI CONN

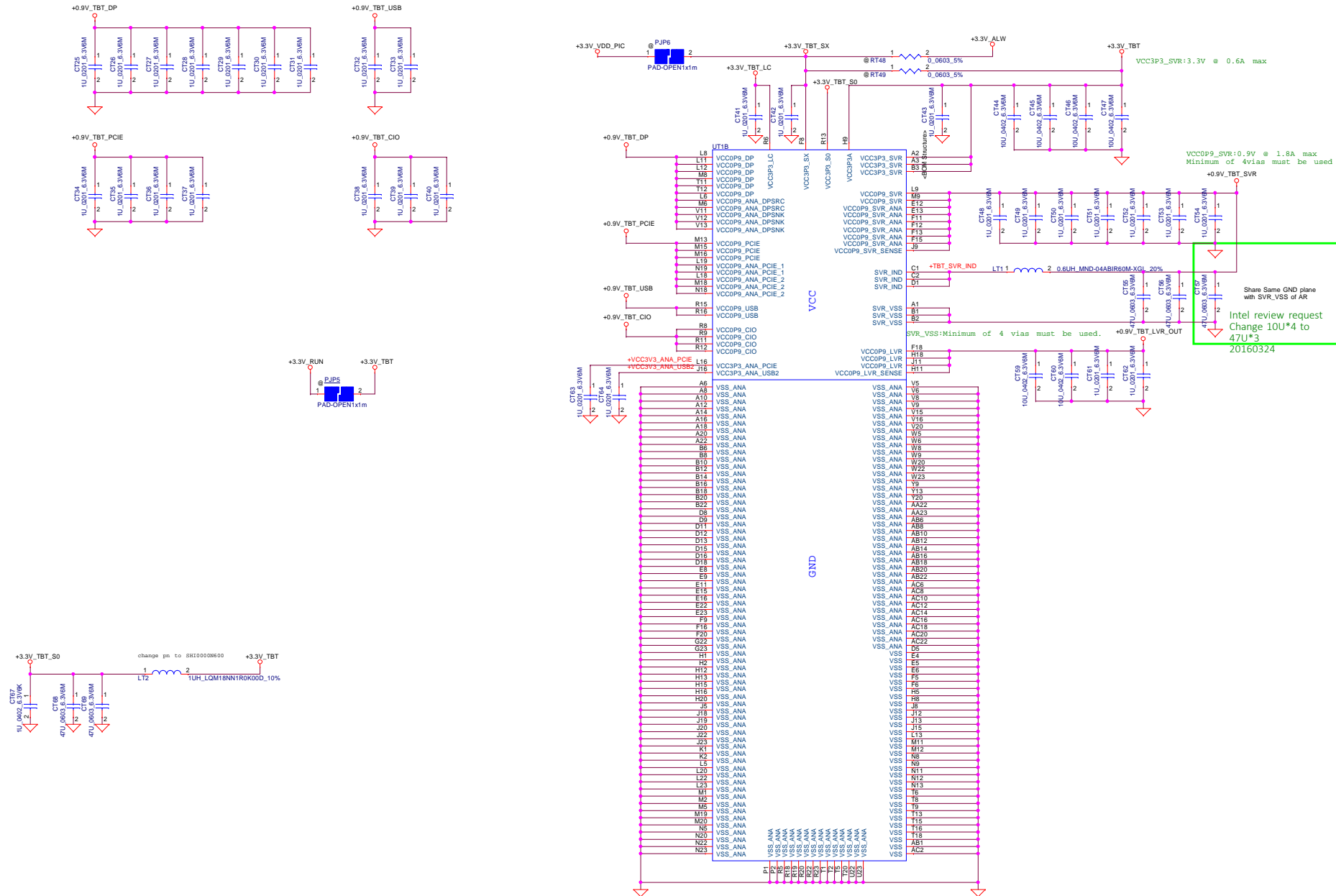
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Title **TBT-AR-SP(2/2) PWR,VSS**

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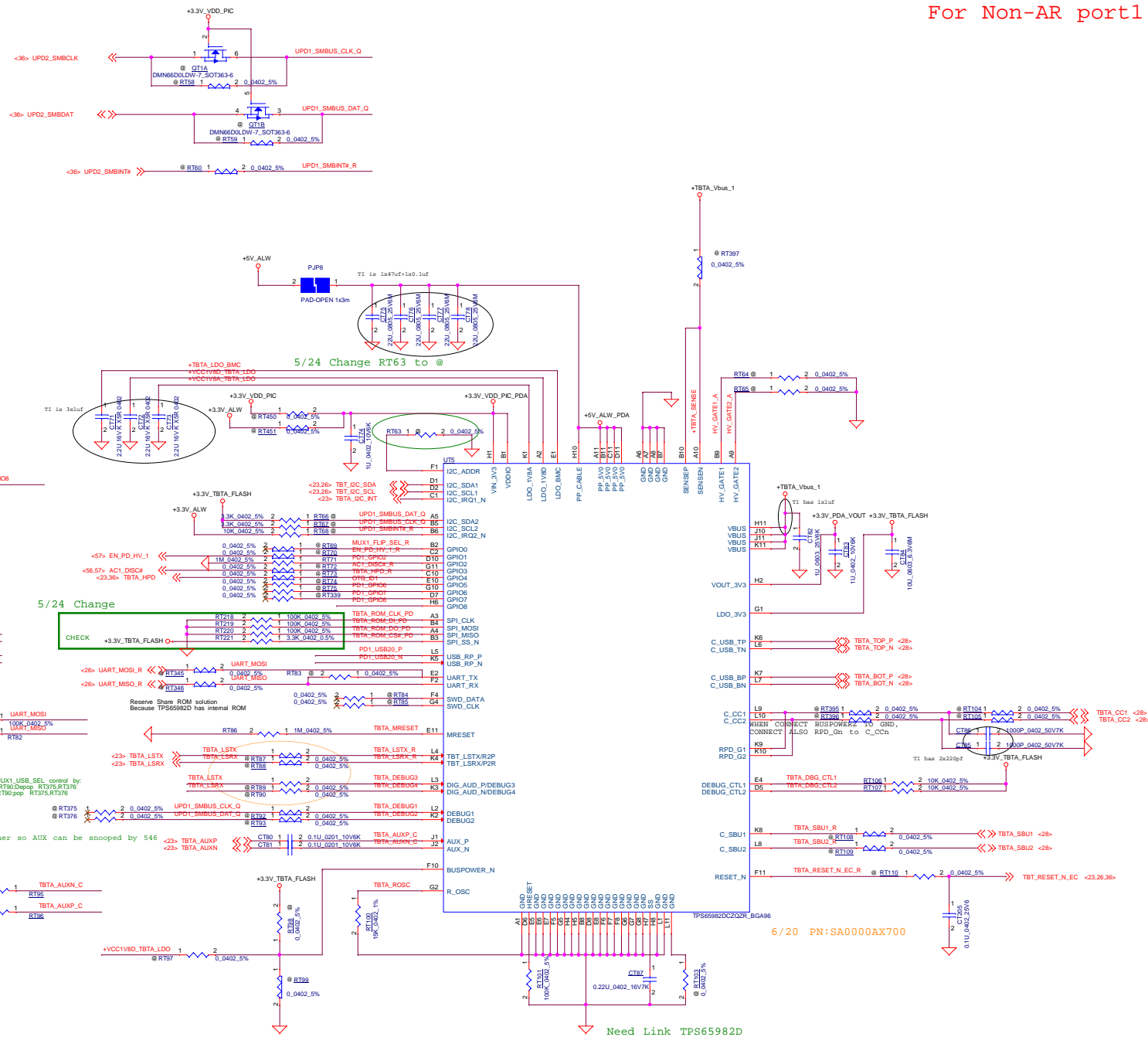
LA-F292P

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For Non-AR port1

5/24 Change ROM From TBTA to TBTB

5/24 Del FLASH Conn.



Div = R2/(R1+R2)		Factory Configuration	Device Configuration	Description
Div_min	Div_max			
0.00	0.08	0		UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.16	1		UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configurations TI VID supported
0.20	0.28	2		UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3		UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configurations TI VID supported
0.40	0.48	4		DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5		DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. <i>Accepts data role swaps to UFP and can initiate.</i>
0.60	0.68	6		DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. <i>Accepts data role swaps to DRP and can initiate.</i>
0.70	1.00	7		Infinite boot retry from Flush to Host IF0 cycles.

Need Link [TPS65982D](#)

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**[Type C]PD Controller TI**

LA-F292F

Rev	1
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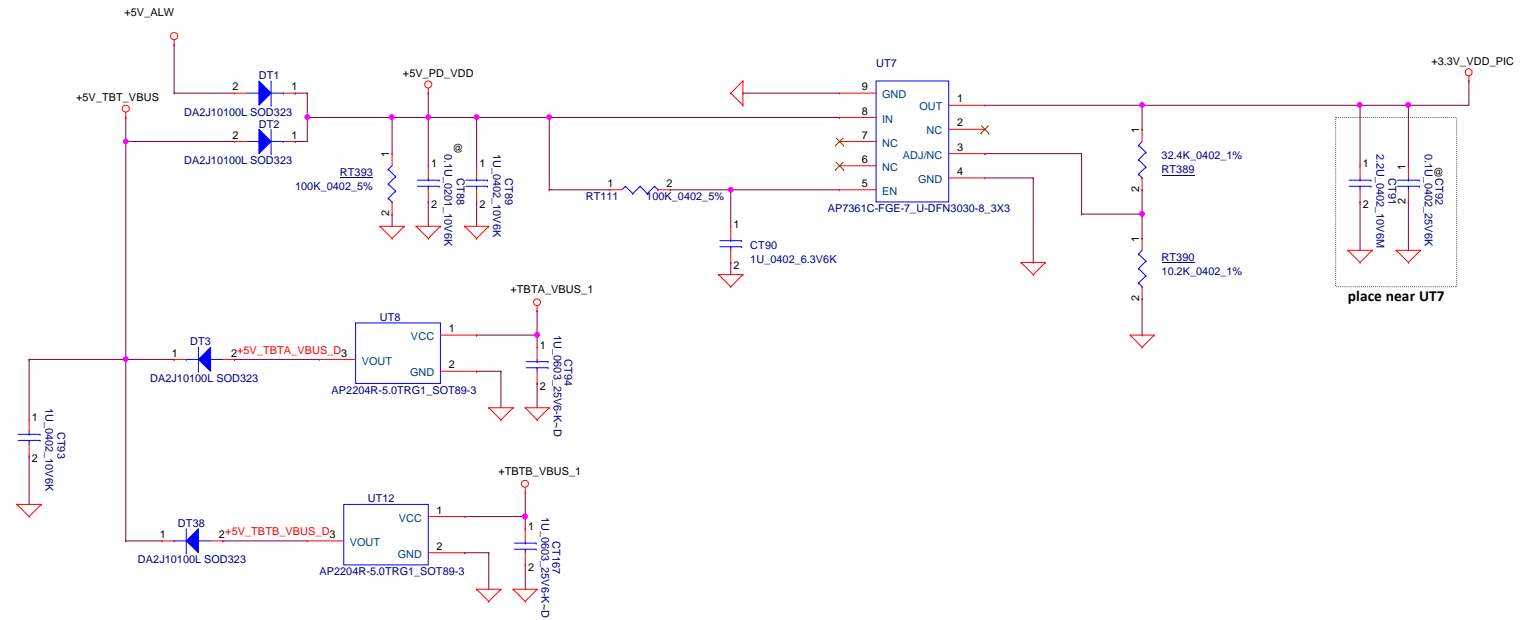
Date: Tuesday, November 14, 2017 Sheet 25 of 6

0.70	1.00	7	Infinite boot retry from Flash to Host VF cycles.
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For kirkwood



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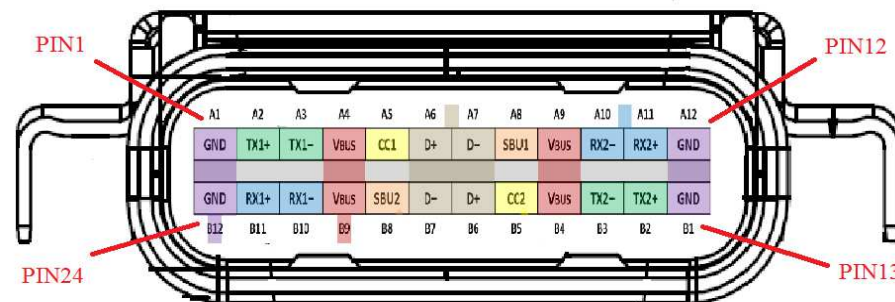
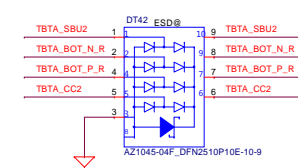
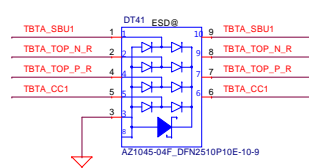
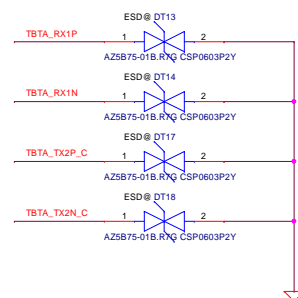
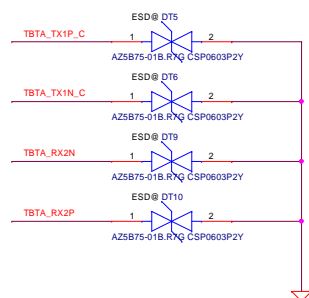
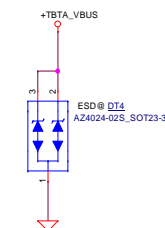
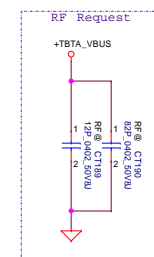
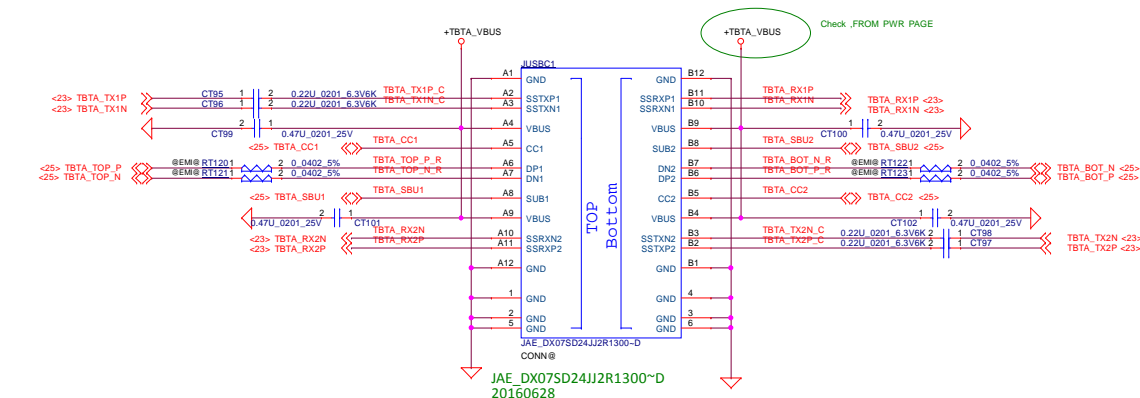
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Title			
[Type C]PD Power-2			
LA-F292P			
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Rev  
1.0

For NON AR Config

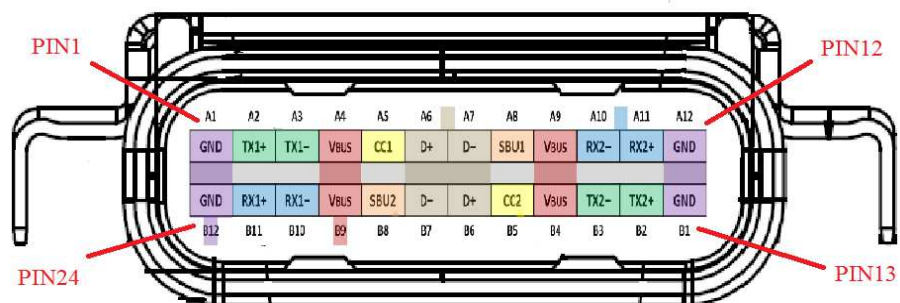
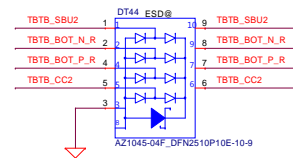
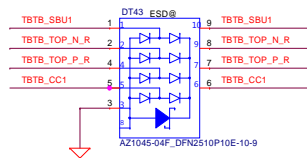
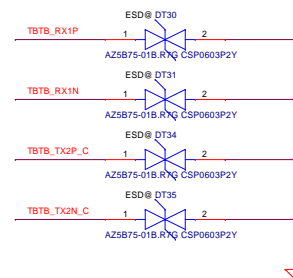
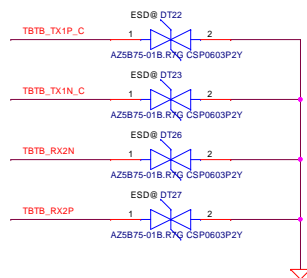
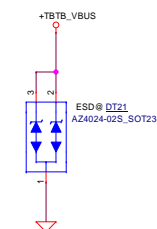
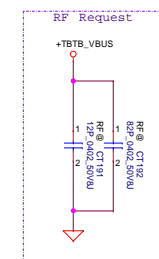
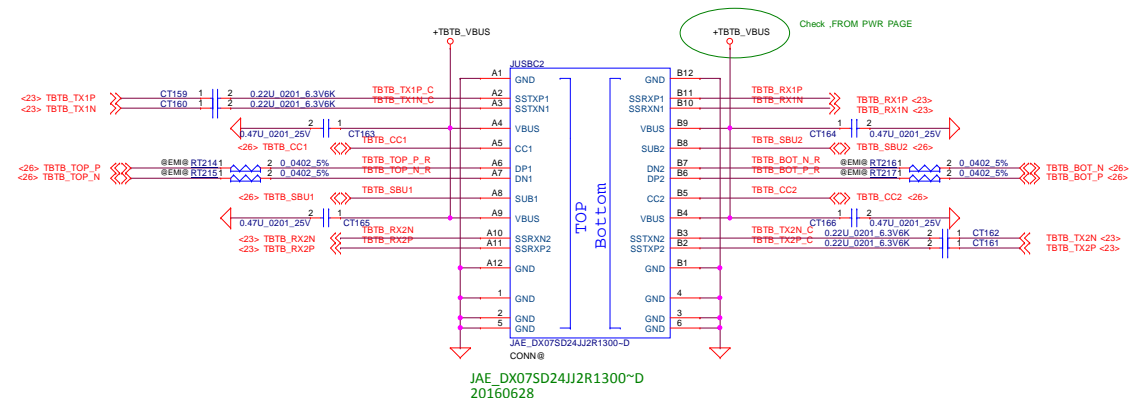
Rear Side



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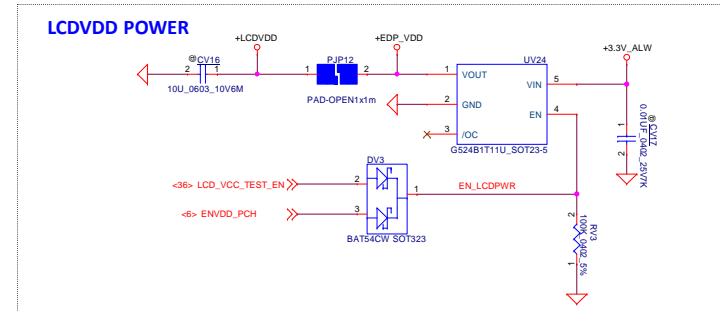
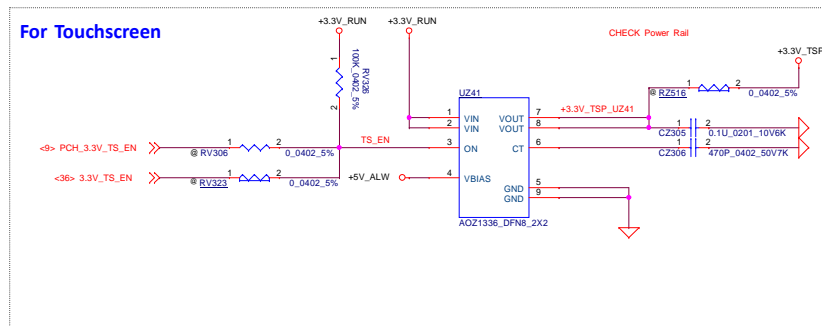
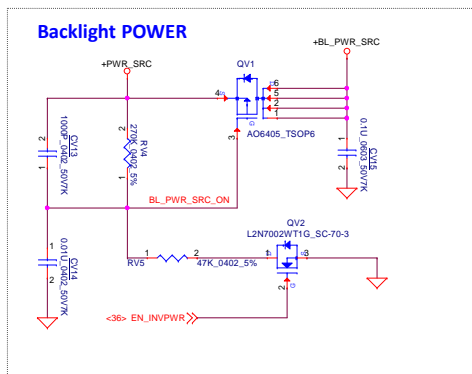
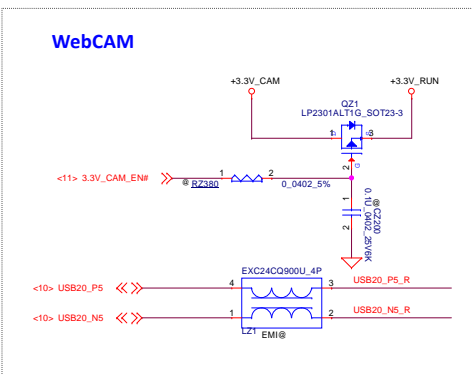
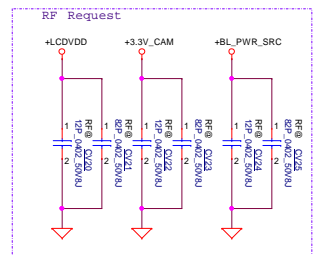
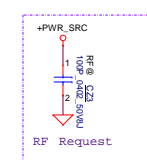
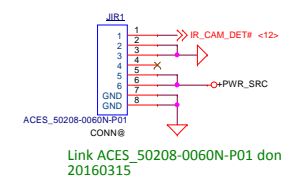
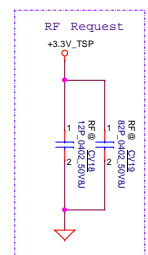
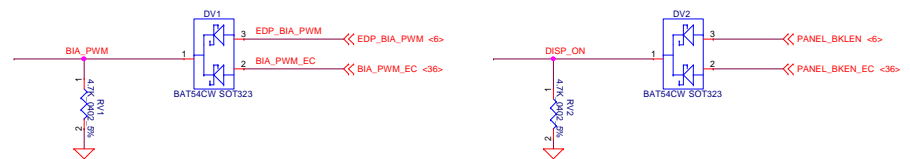
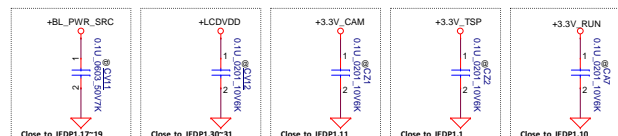
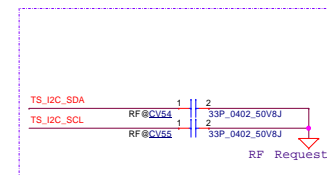
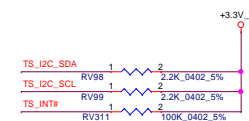
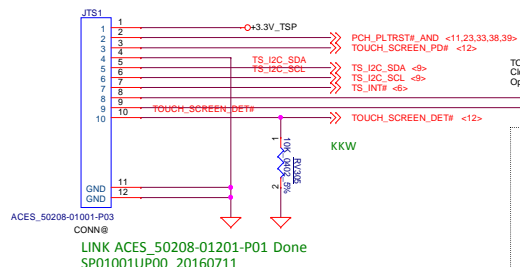
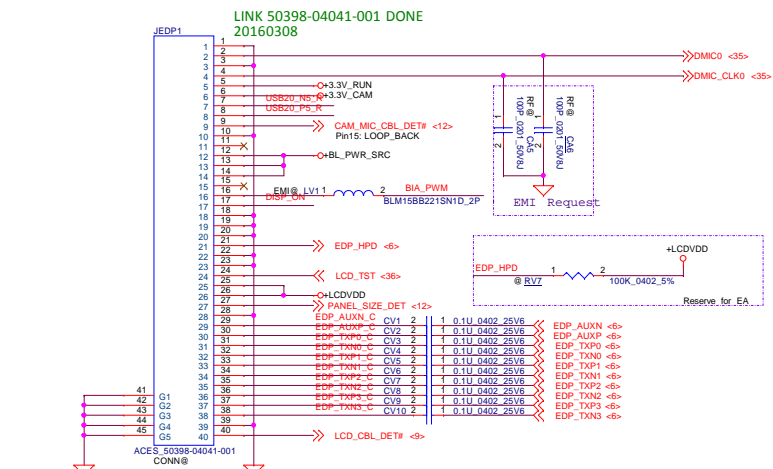
Compal Electronics, Inc.			
USB 3.0 CONN TYPE C			
LA-F292P			
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For kirkwood  
For NON AR Config  
Front Side



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Size	Document Number	Rev	
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Date:	Tuesday, November 14, 2017	Sheet	29 of 60

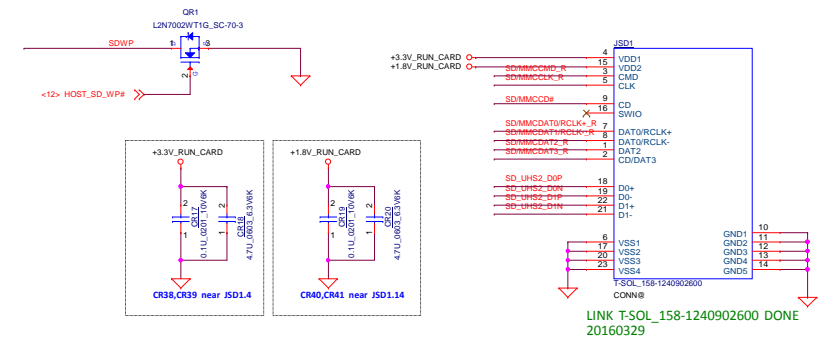


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Compal Electronics, Inc.	
eDP CONN & Touch screen	
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<b>Compal Electronics, Inc.</b>			
	Title		
	<b>Card Reader RTS5330</b>		
	Size	Document Number	Rev
		<b>LA-F292P</b>	<b>1.0</b>

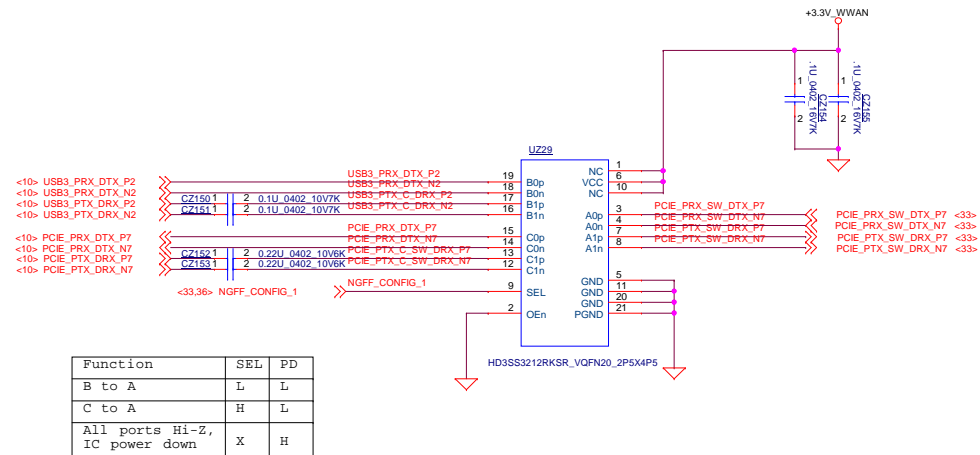


HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)

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## PCIE/USB MUX


NEED LINK TI HD3SS3212 as main



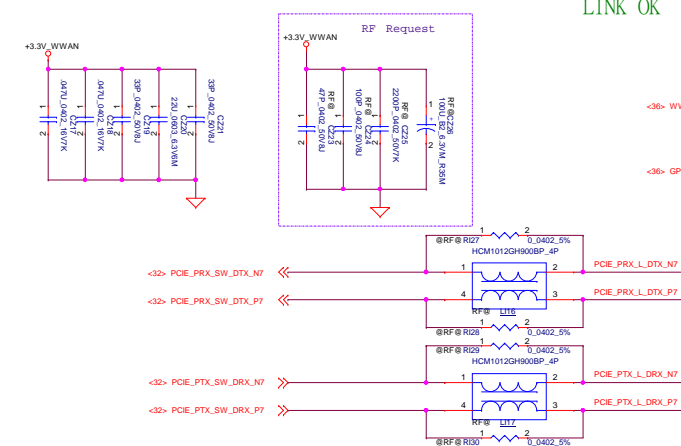
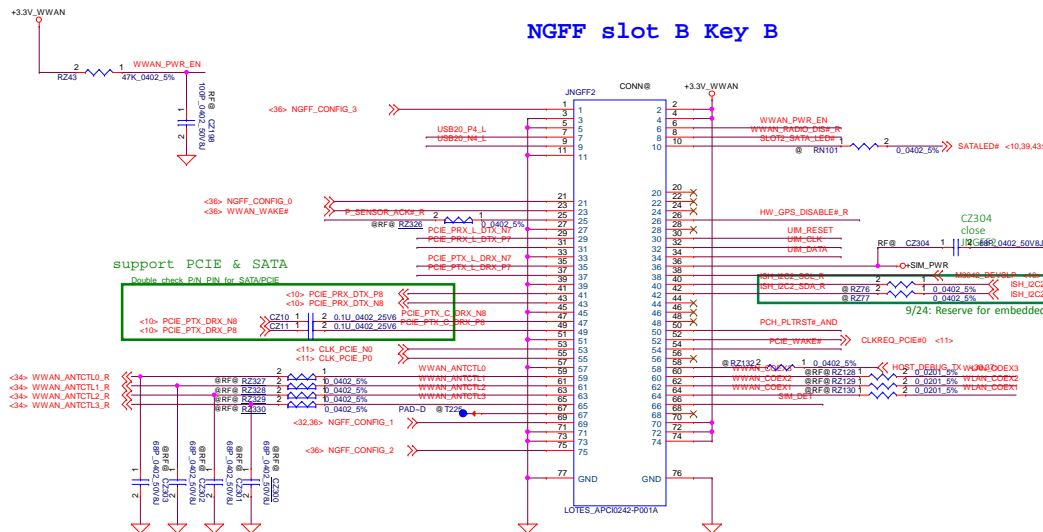
STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	HIGH
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	LOW
8	HIGH	GND	GND	GND	WWAN	LOW
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	LOW
15	HIGH	HIGH	HIGH	HIGH	NA	LOW

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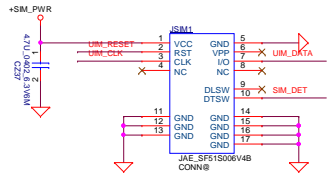
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	Compal Electronics, Inc.		
	USB/PCIE MUX		
	LA-F292P		
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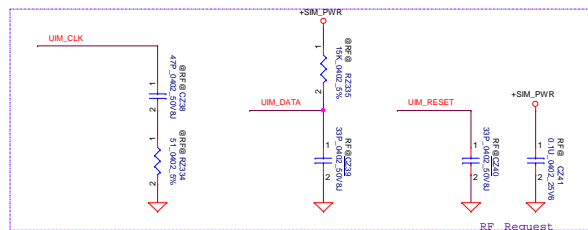




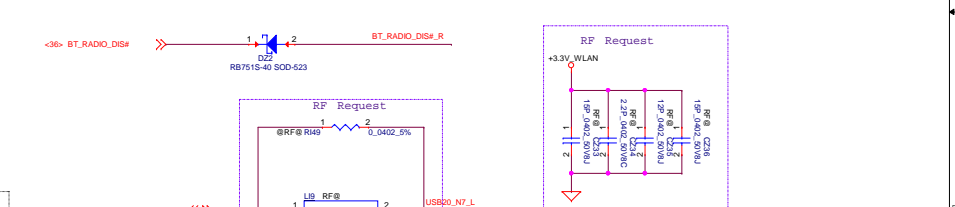
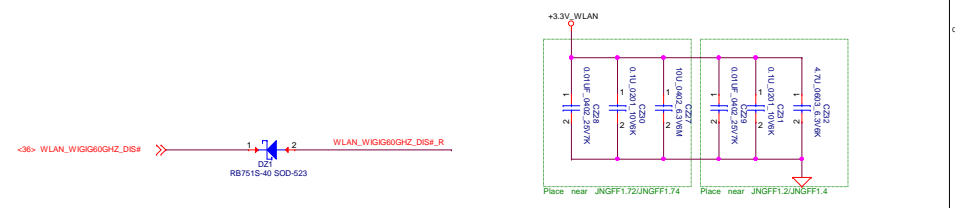
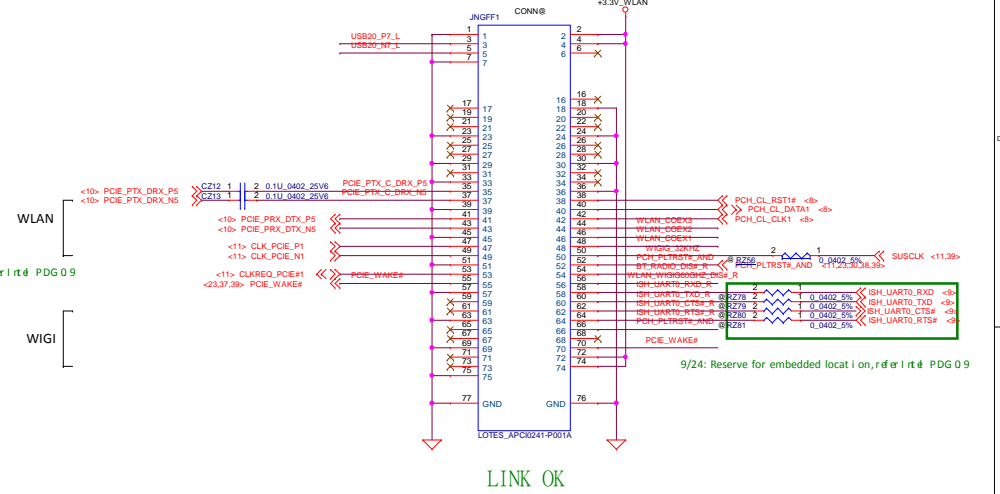
### SIM Card Push-Push



JAE\_SF51S006V4DR1000Q LINK DONE  
20160321 (Temp symbol is correct, SP number is wrong on DTSW)



### NGFF slot A Key A Only for Kirkwood 80148-3221&80148-4221 Footprint the same



### Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power	Aux Power
+3.3V		Peak	Normal

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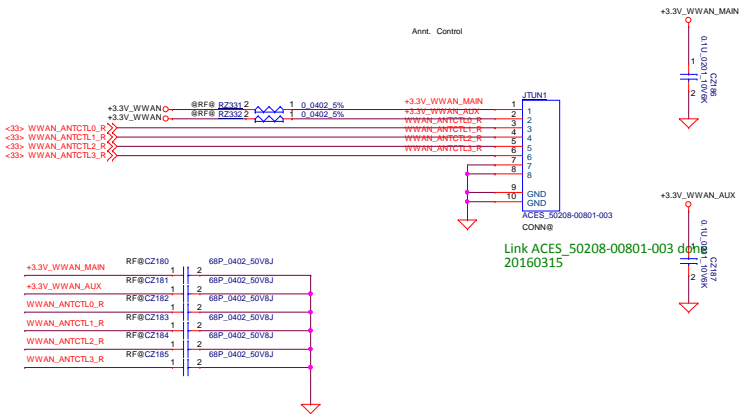
NGFF Card

LA-F292P

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Only for Kirkwood



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### Internal Speakers Header

40 mils trace keep 20 mil spacing

INT-SPKR-L+ INT-SPKR-L- INT-SPKR-R+ INT-SPKR-R- INT-SPKR-L+ INT-SPKR-L- INT-SPKR-R+ INT-SPKR-R-

BLM16PXX33SN1D 2P BLM16PXX33SN1D 2P BLM16PXX33SN1D 2P BLM16PXX33SN1D 2P

EM16 LA6 EM16 LA7 EM16 LA8 EM16 LA9

EM16 CA4 EM16 CA5 EM16 CA6 EM16 CA7 EM16 CA8 EM16 CA9

10000 OHM 50V/K 10000 OHM 50V/K 10000 OHM 50V/K 10000 OHM 50V/K 10000 OHM 50V/K 10000 OHM 50V/K

Close to UA1

ACE50278-00601-20160325

INT-SPKR-L+ INT-SPKR-L- INT-SPKR-R+ INT-SPKR-R- INT-SPKR-L+ INT-SPKR-L- INT-SPKR-R+ INT-SPKR-R-

1 2 3 4 5 6

SPK\_DET#

Change to 6pin to support Link ACE50278-00601-20160325

+3.3V\_RUN

DMIC\_CLK0

Add for solving pop noise and detect issues

Reserve for support D3 cold

RE313@one control line if DVDD is 3.3  
DE2@two control lines1

Diagram illustrating the microphone layout for HP and Nokia devices. The HP side shows 'HP-Out-Right' and 'HP-Out-Left' microphones. The Nokia side shows 'Nokia-MIC' and 'iPhone-M' microphones.

Global Headset  
**Universal Jack**

Normal

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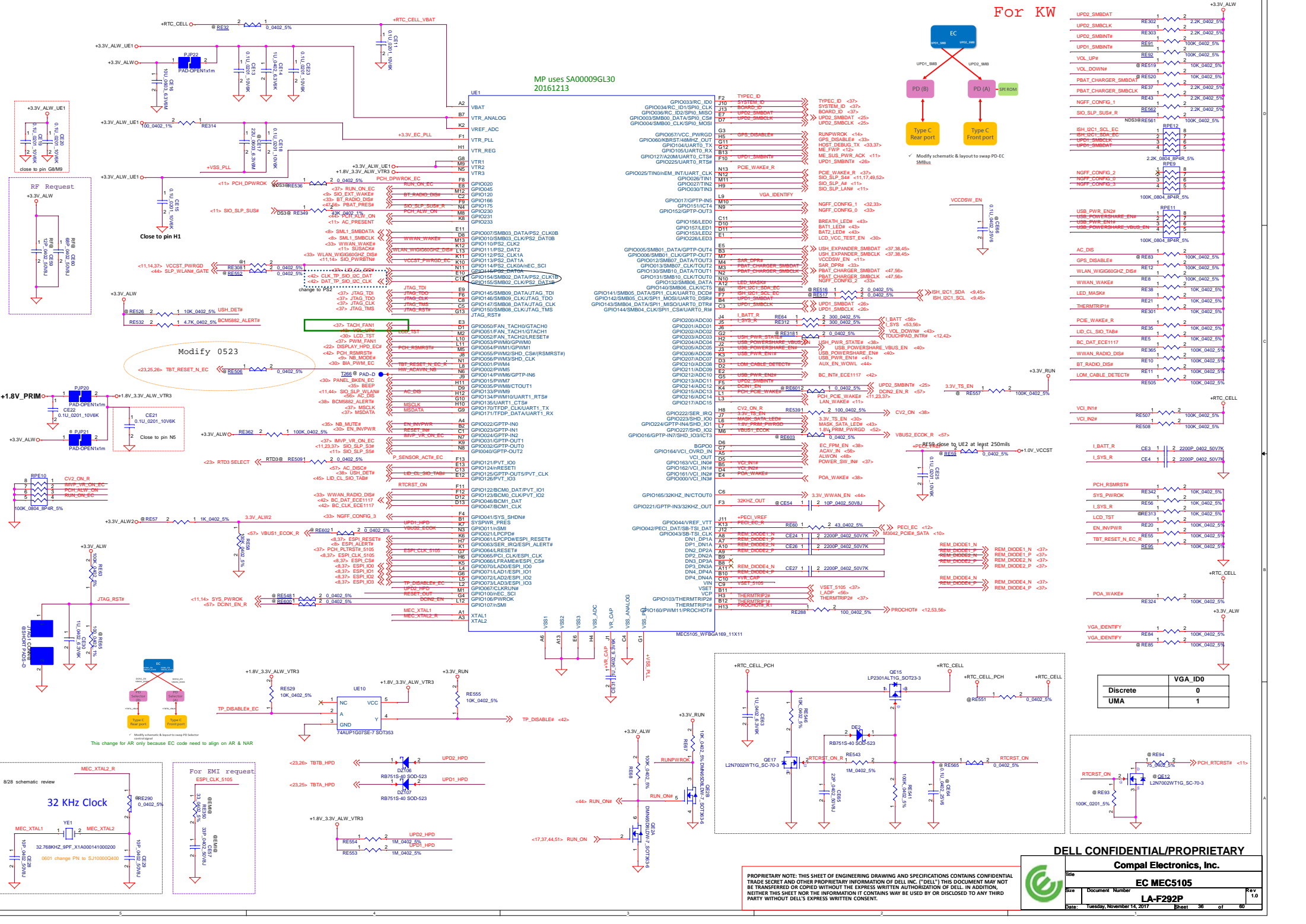
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**Compal Electronics, Inc.****Codec ALC3253**

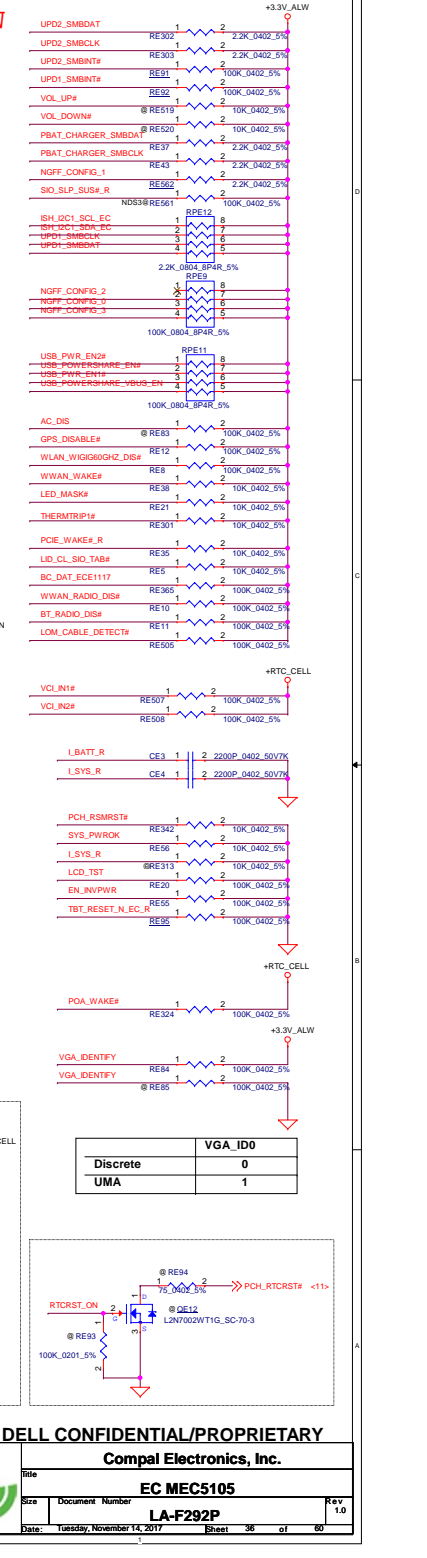
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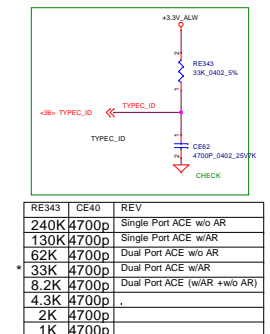
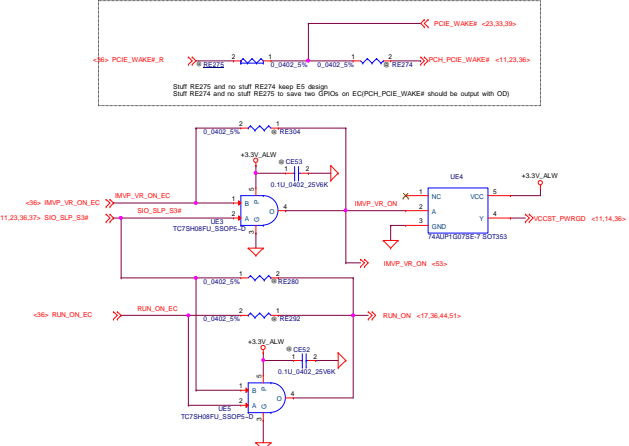
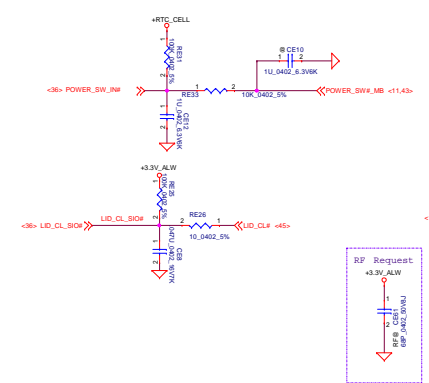
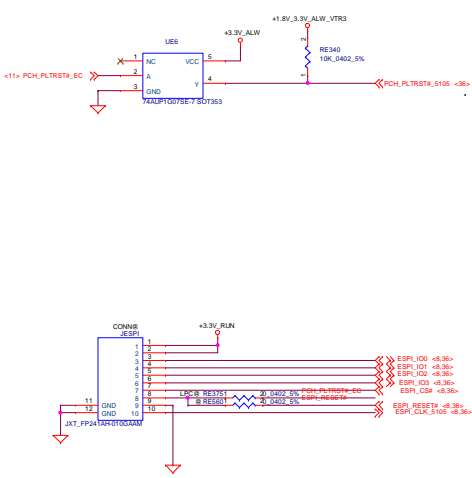
LA-P292P

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For KW





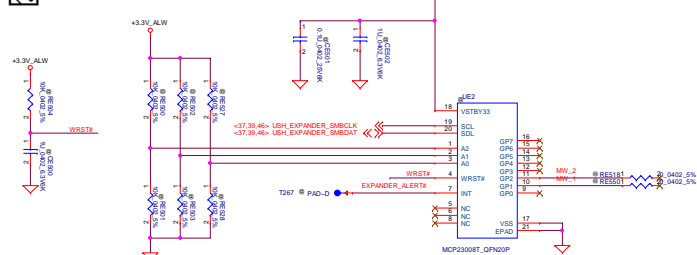
RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	Reserve
4.3K	4700p	A00
2K	4700p	
1K	4700p	

RE300	CE47	PANEL SIZE
240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
33K	4700p	14"
8.2K	4700p	15"
4.3K	4700p	17"
2K	4700p	15P
1K	4700p	

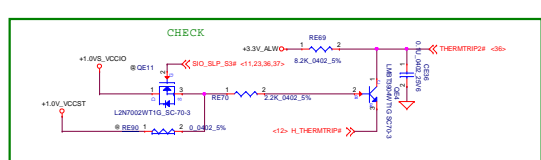
Control Byte							
5	1	0	0	A2	A1	A0	R/W

R/W = 0 = Write  
R/W = 1 = Read

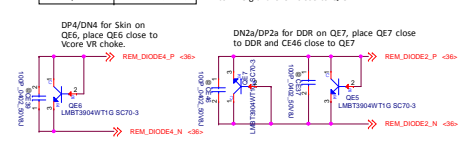
SMBus address 0x40



Link MCP23008 OK

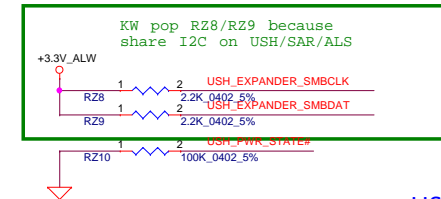
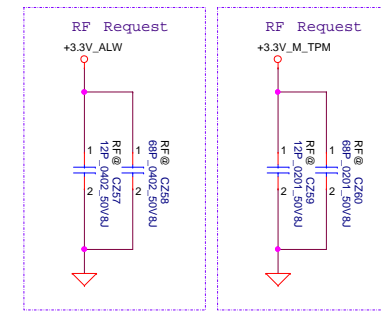
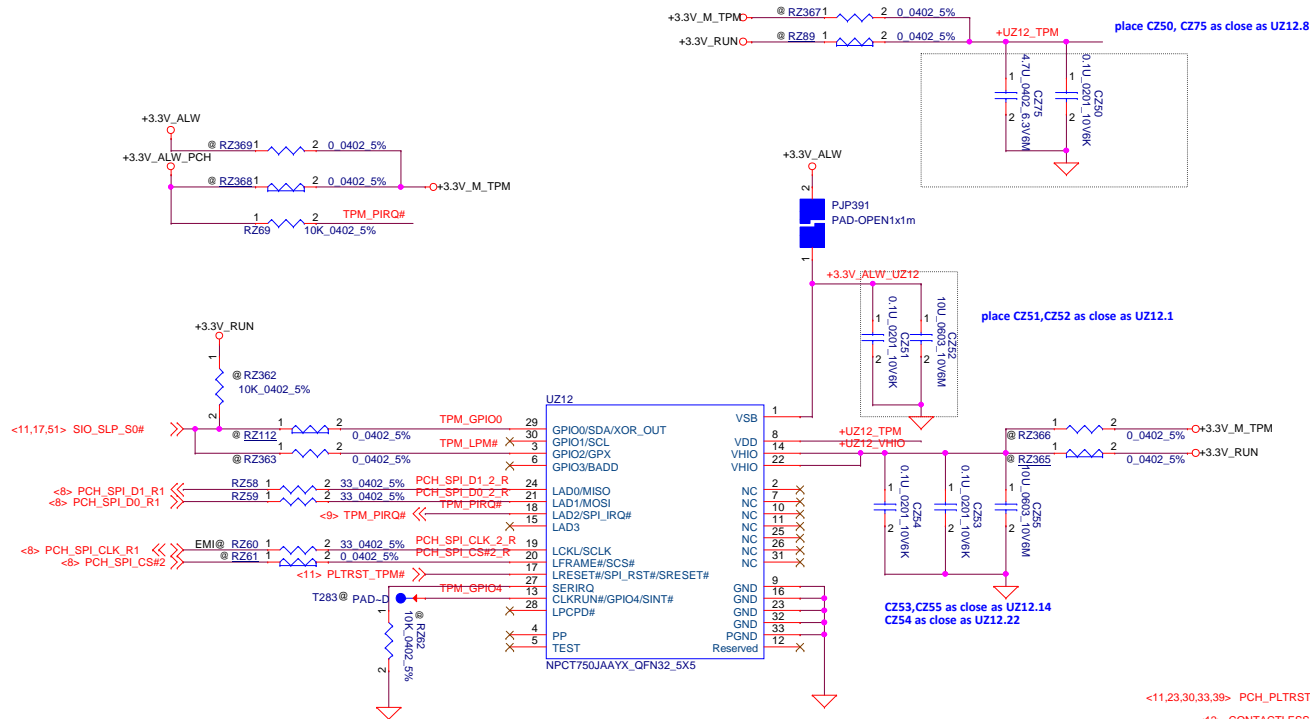


Thermal diode mapping	
5085 Channel	Locat i on
DP1/DN1	CPU (QE3)
DP2/DN2	AR (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

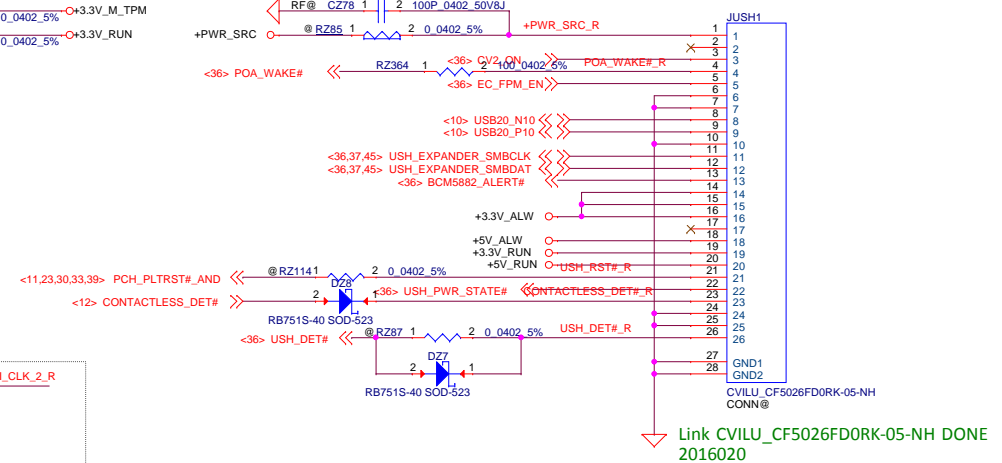


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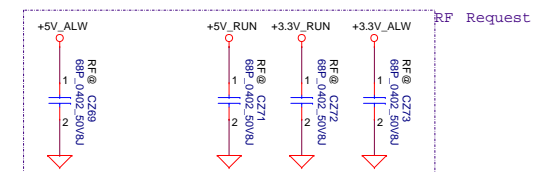
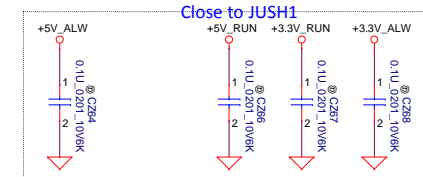
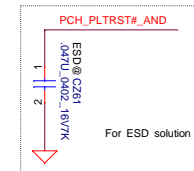
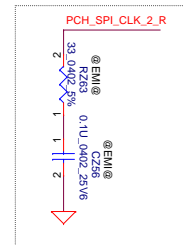
For NUVOTON TPM



USH CONN



	Pop	Depop	Comment
NPCT65x	RZ89, RZ366, RZ62, RZ363	RZ365, RZ367, RZ112	VDD - V_RUN Power VHIO - V_SPI Power
NPCT75x	RZ89, RZ365, RZ112	RZ367, RZ366, RZ62, RZ363	Option1 (recommended) VDD and VHIO - V_RUN power
NPCT75x	RZ367, RZ366	RZ89, RZ365, RZ62	Option2 (for Z1 sample [early sample]) VDD and VHIO - V_SPI power



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## USH & TPM

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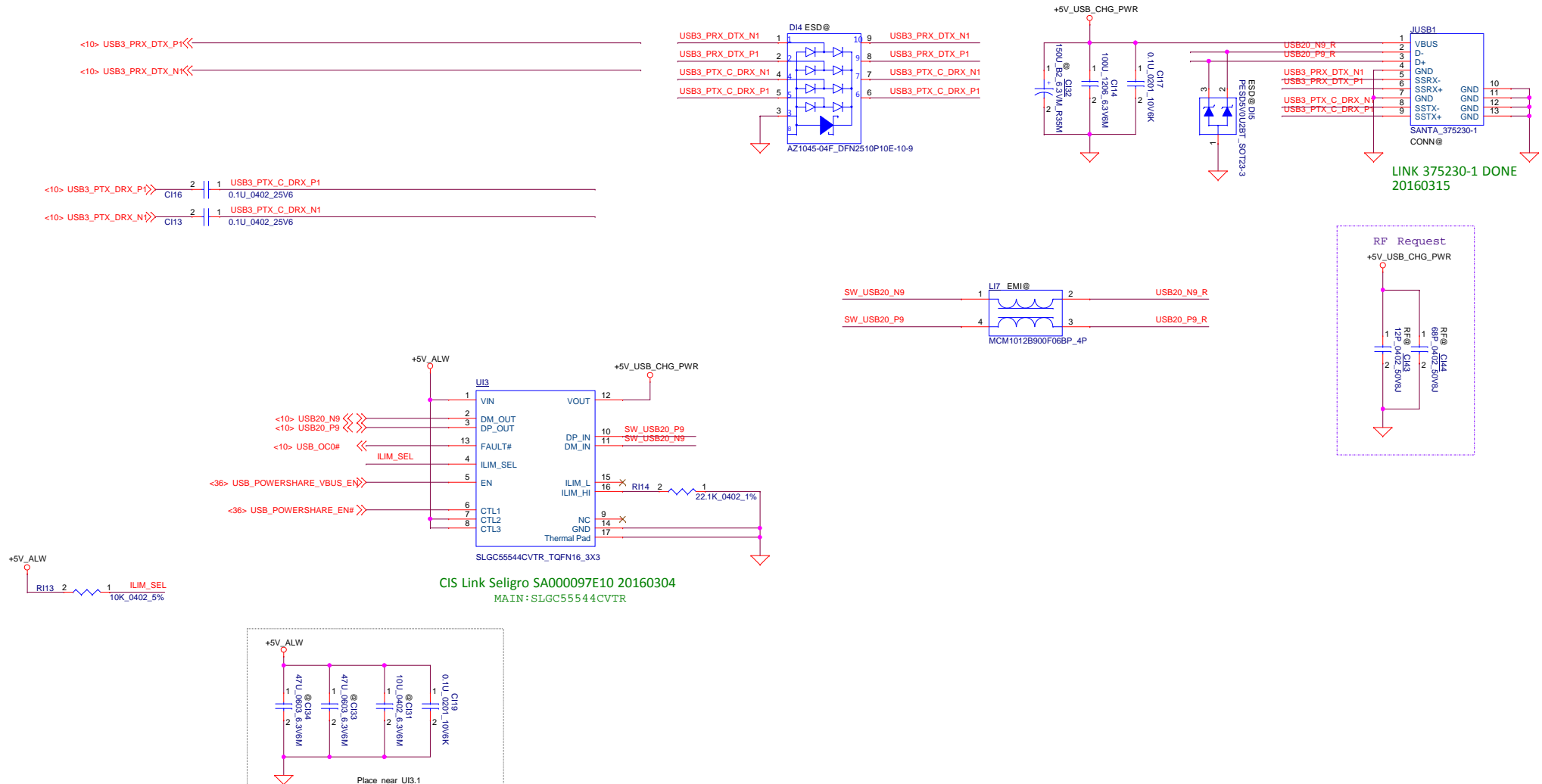
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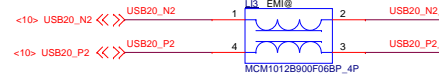
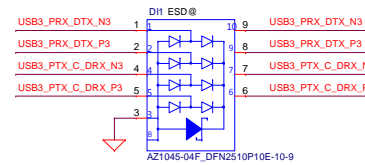


# For PWR SW + Charger combine IC

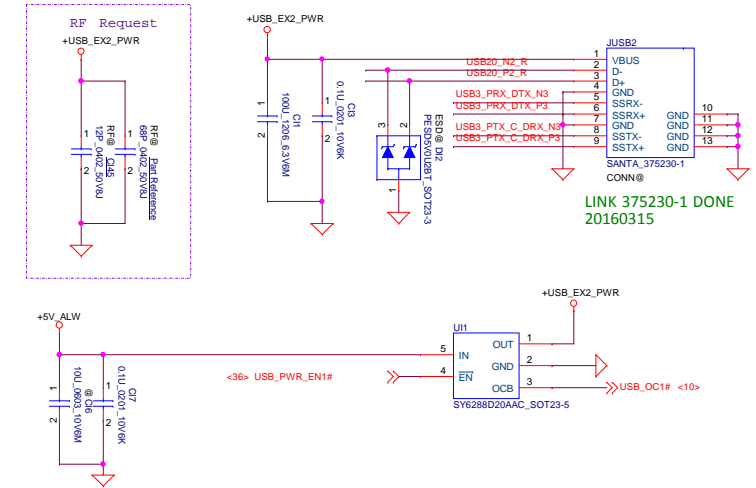
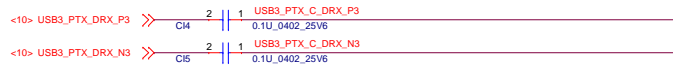


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Compal Electronics, Inc.			
Title <b>JUSB1+PS</b>			
Size	Document Number	Rev	
	<b>LA-F292P</b>	1.0	
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```
DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm
```



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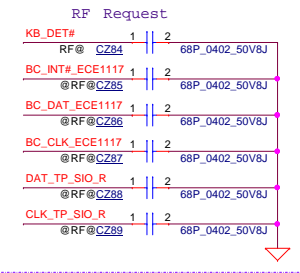
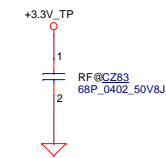
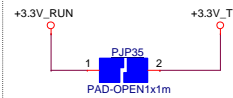
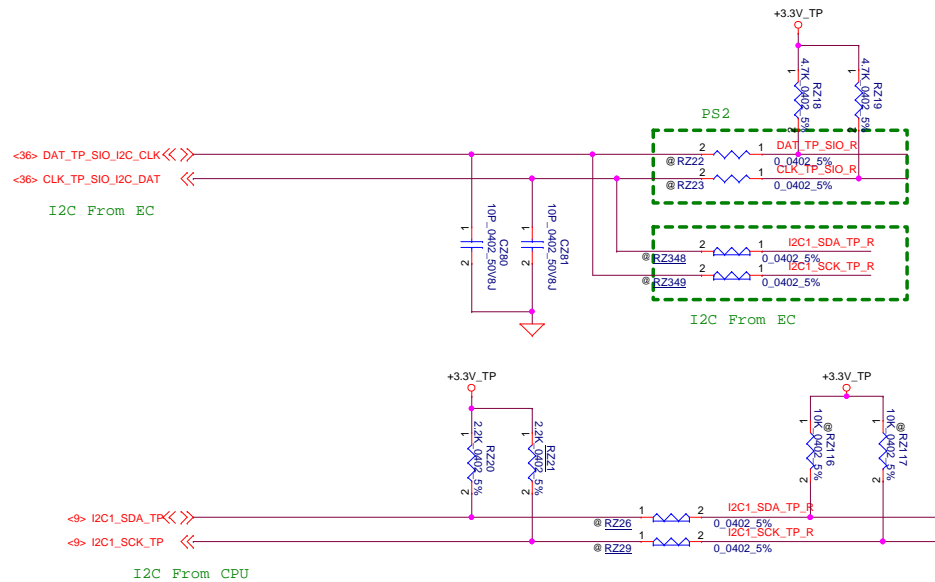
**Compal Electronics, Inc.**



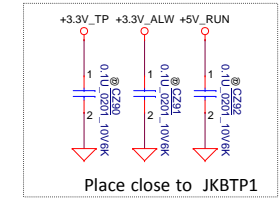
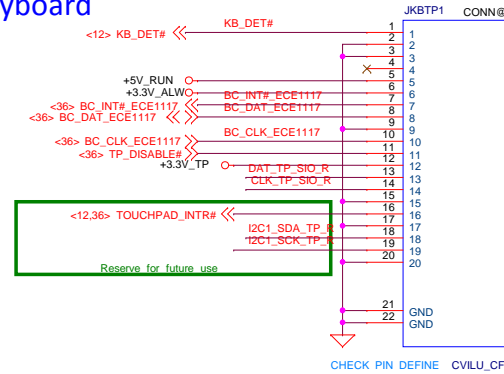
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<b>JUSB2</b>			
Size	Document Number	Rev	
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## Touch Pad

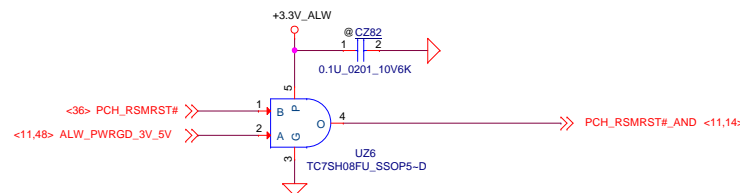


## Keyboard



Link CVILU\_CF5020FD0R0-05-NH DONE  
20160321

## RSMRST circuit



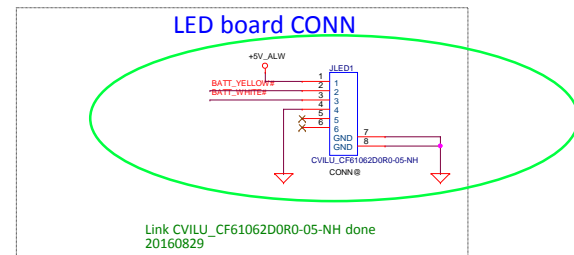
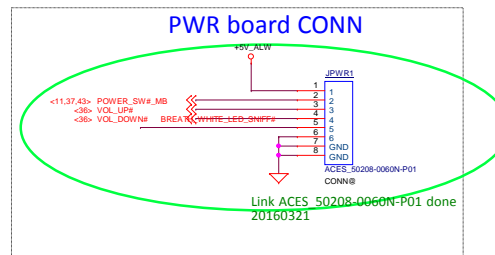
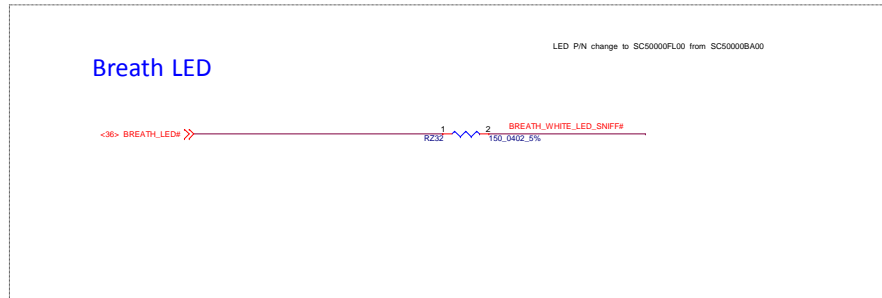
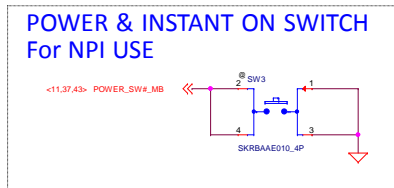
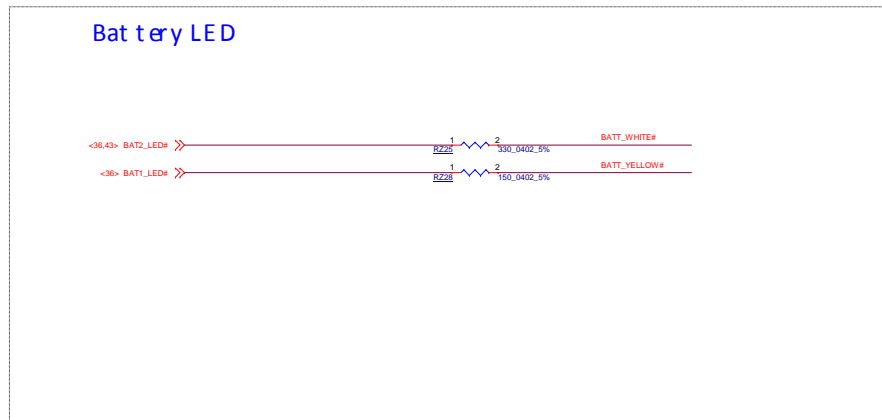
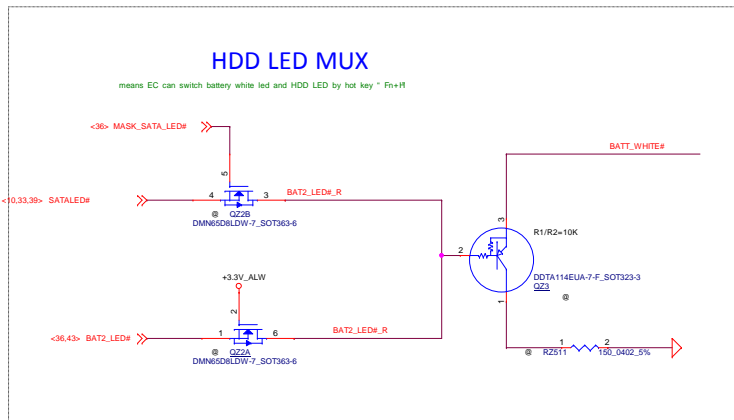
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#### Fiducial Mark

- FD1: FIDUCIAL MARK-D
- FD2: FIDUCIAL MARK-D
- FD3: FIDUCIAL MARK-D
- FD4: FIDUCIAL MARK-D

#### LED Circuit Control Table

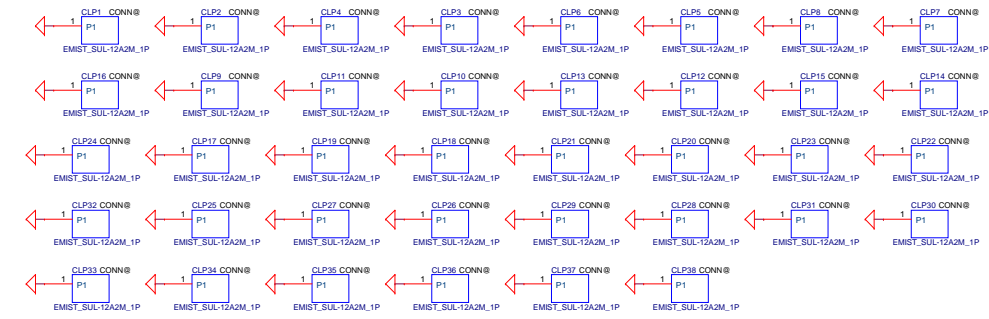
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask CPUs (Lid Opened)	1	1

#### For JAE JSIM1 boss hole

#### CPU

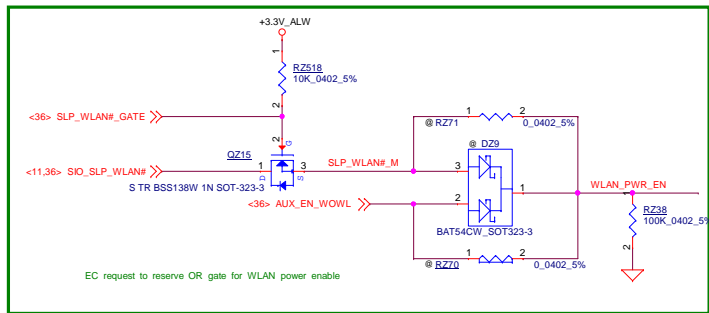
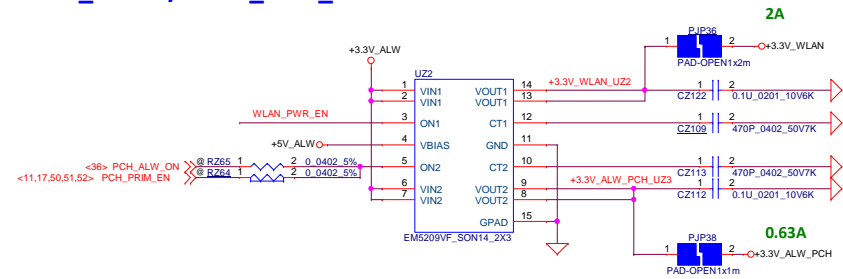
#### NGFF

#### EDP screw-hole

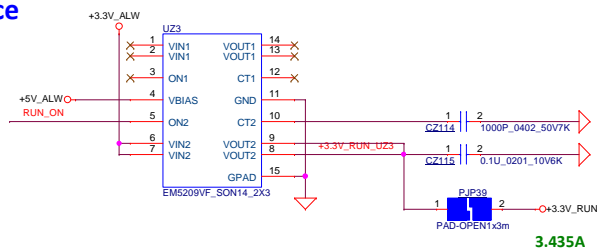


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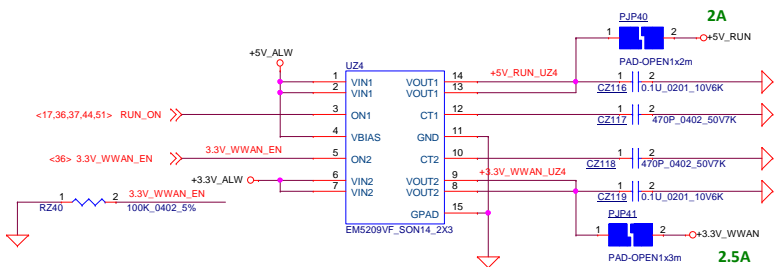
### +3.3V\_WLAN/+3.3V\_ALW\_PCH source



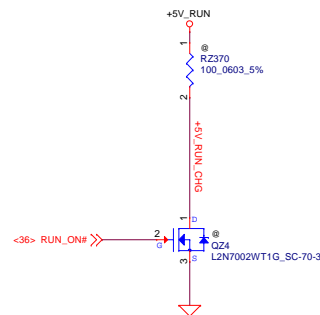
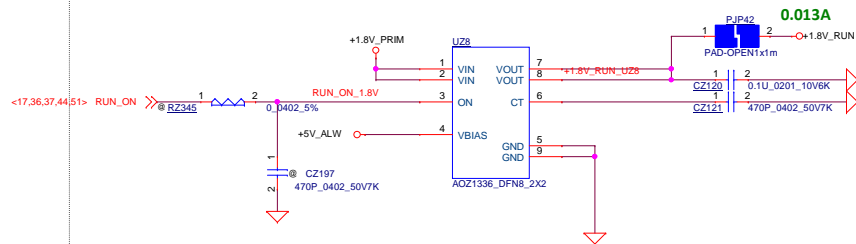
### +3.3V\_RUN source



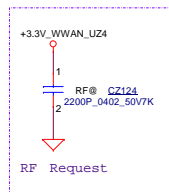
## +5V\_RUN/+3.3V\_WWAN source



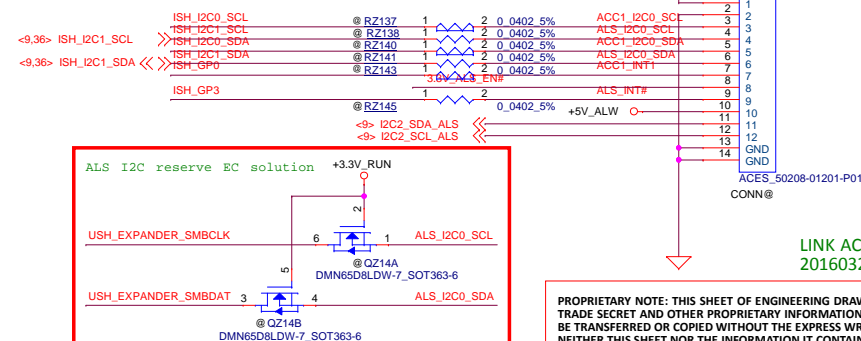
## +1.8V\_RUN source



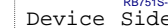
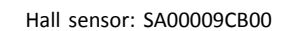
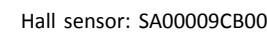
Reserve for S3 no power issue (+5V\_RUN discharge circuit)



## SAR Sensor



Located near the WWAN antenna



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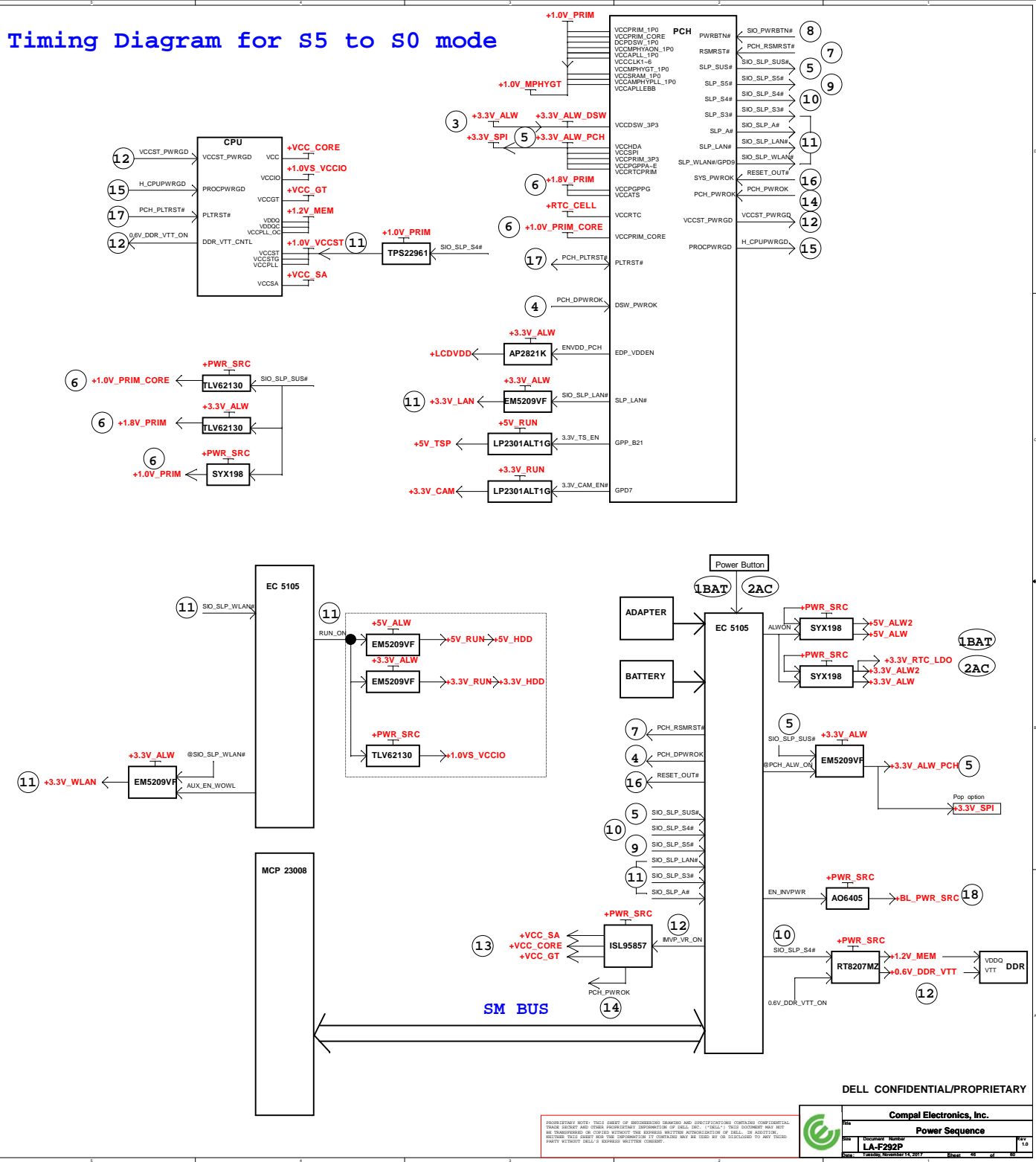
## SENSOR

**LA-F292P**

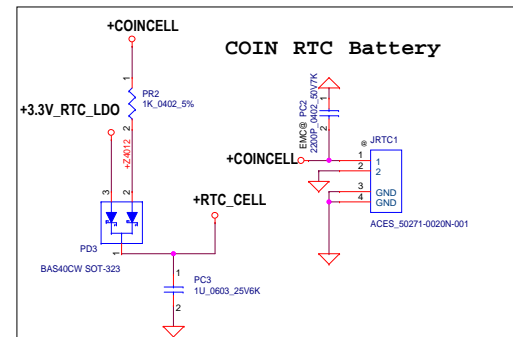
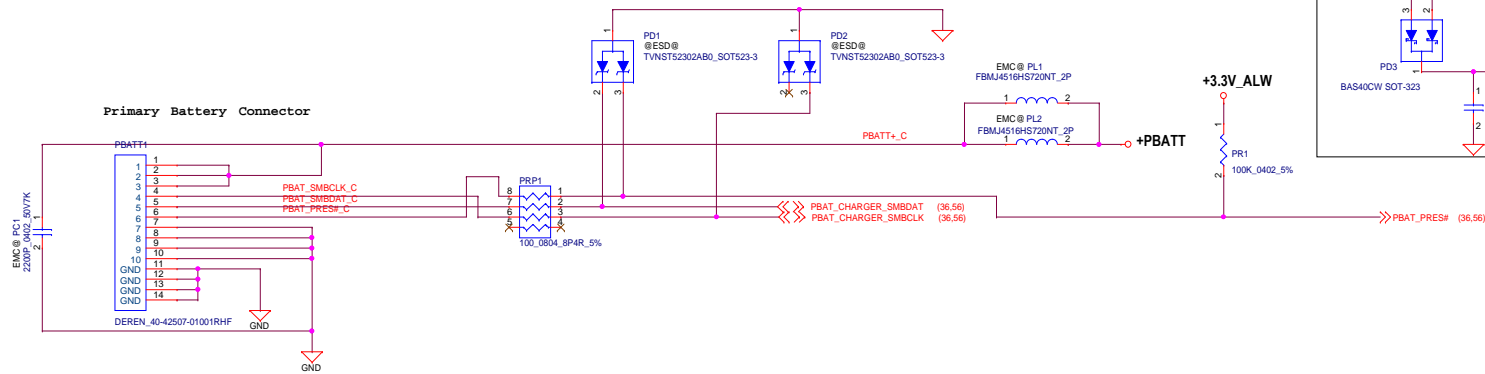
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### Timing Diagram for S5 to S0 mode







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		BATT/RTC	
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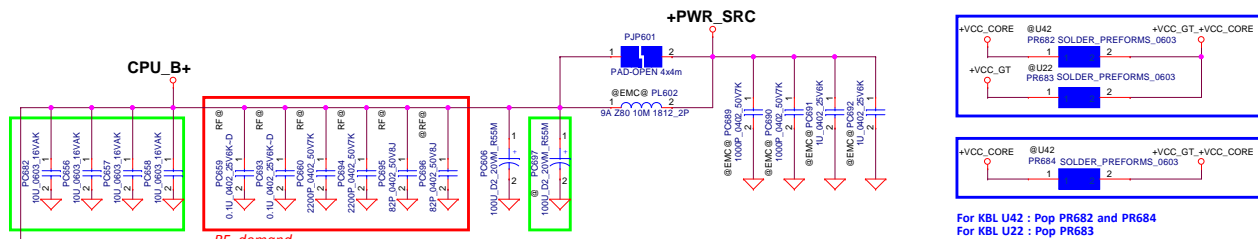












## AR U42

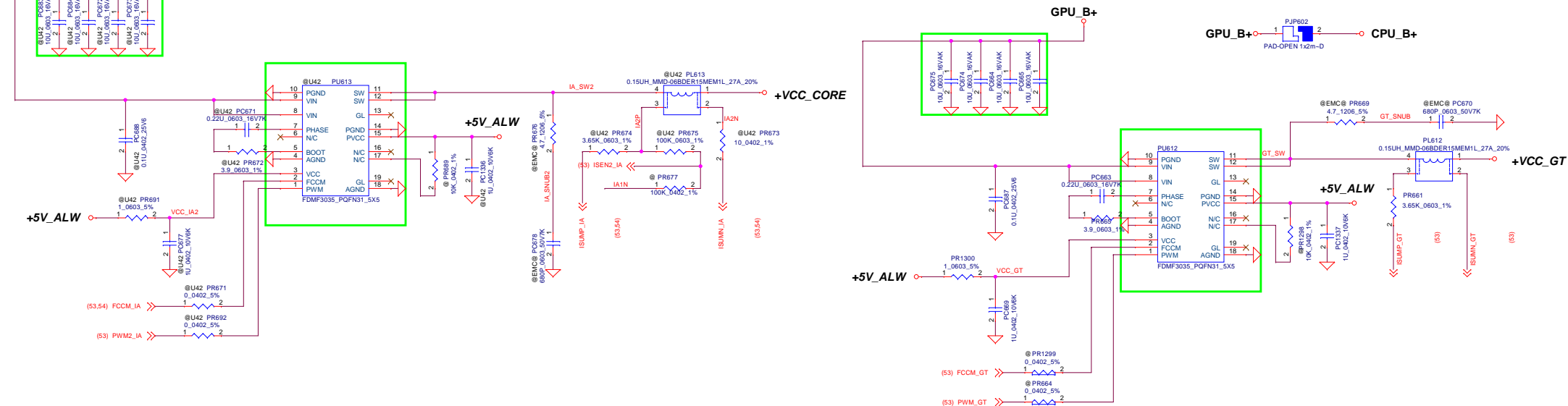
PC826 @U42AR 0.1U_0402_25V6	PR813 @U42AR 93.1K_0402_1%	PR621 @U42AR 1K_0402_1%	PC817 @U42AR 220P_0402_50V7K	PC824 @U42AR 0.01UF_0402_25V7K	PC642 @U42AR 0.022U_0402_16V7K	PR651 @U42AR 113K_0402_1%
PR638 @U42AR 453_0402_1%	PR622 @U42AR 3.09K_0402_1%	PC616 @U42AR 68P_0402_50V8J	PR636 @U42AR 732_0402_1%	PC646 @U42AR 0.047U_0402_25V7K	PR629 @U42AR 86.6K_0402_1%	PR617 @U42AR 4.3K_0402_1%

## nAR U42

PC826 @U42NAR 0.1U_0402_25V6	PR813 @U42NAR 93.1K_0402_1%	PR621 @U42NAR 1K_0402_1%	PC817 @U42NAR 220P_0402_50V7K	PC824 @U42NAR 0.022U_0402_16V7K	PC642 @U42NAR 0.022U_0402_16V7K	PR651 @U42NAR 105K_0402_1%
PR638 @U42NAR 453_0402_1%	PR622 @U42NAR 3.09K_0402_1%	PC616 @U42NAR 68P_0402_50V8J	PR636 @U42NAR 732_0402_1%	PC646 @U42NAR 0.047U_0402_25V7K	PR629 @U42NAR 88.7K_0402_1%	PR617 @U42NAR 4.3K_0402_1%

## nAR U22

PC826 @U22 0.047U_0402_25V7K	PR813 @U22 88.7K_0402_1%	PR621 @U22 316_0402_1%	PC817 @U22 1200P_0402_50V7K	PC824 @U22 0.022U_0402_16V7K	PC642 @U22 0.022U_0402_16V7K	PR651 @U22 105K_0402_1%
PR638 @U22 360_0402_1%	PR622 @U22 1.5K_0402_1%	PC616 @U22 33P_0402_50V8J	PR636 @U22 732_0402_1%	PC646 @U22 0.047U_0402_25V7K	PR629 @U22 88.7K_0402_1%	PR617 @U22 3.4K_0402_1%

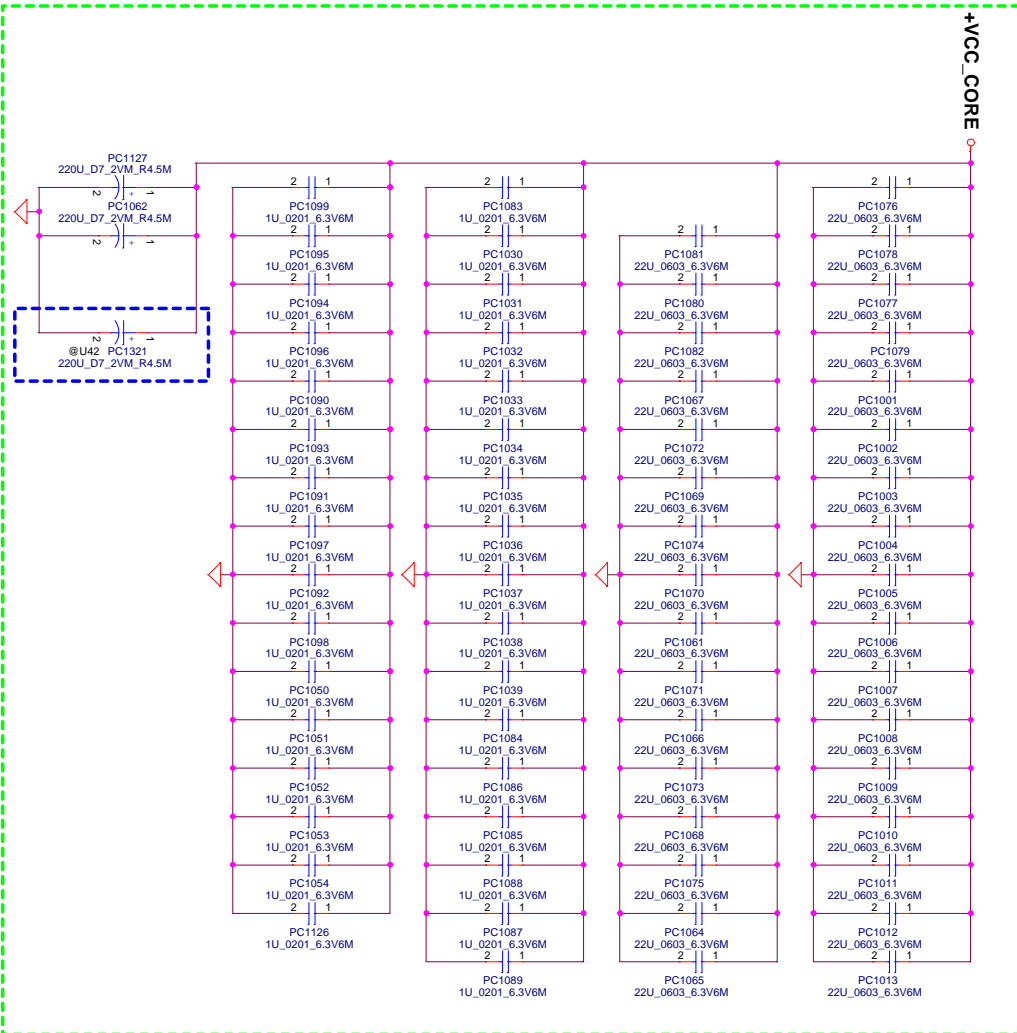


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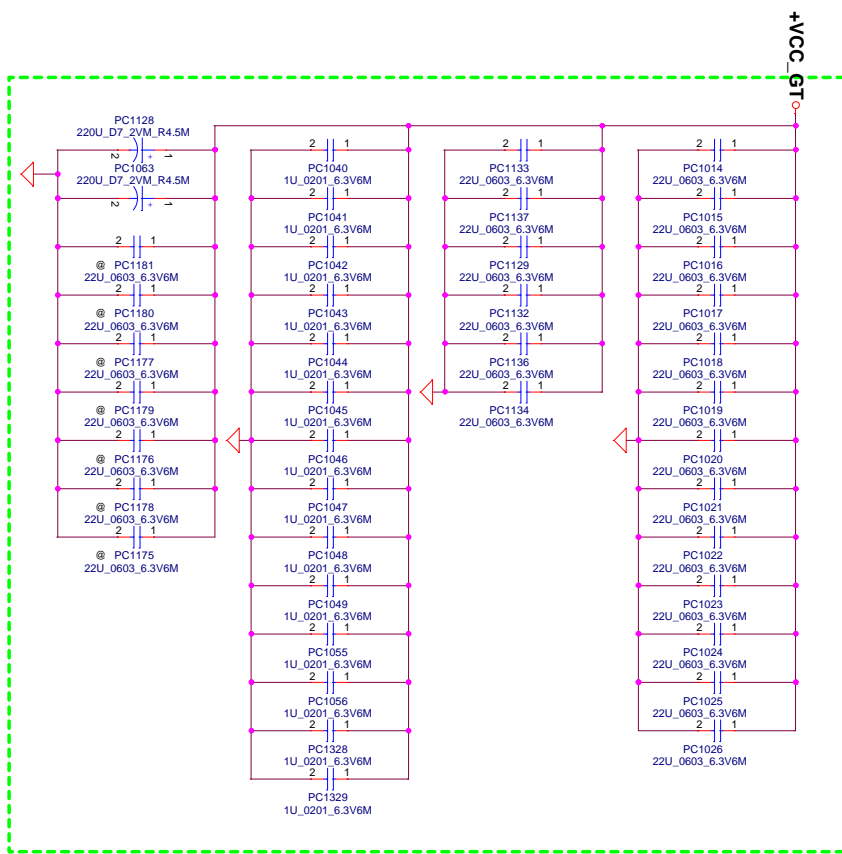
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VCC CORE Place on CPU  
 22U\_0603 \* 33 pcs + 1U\_0201\*33 pcs  
 +220u\_D7\*3 pcs



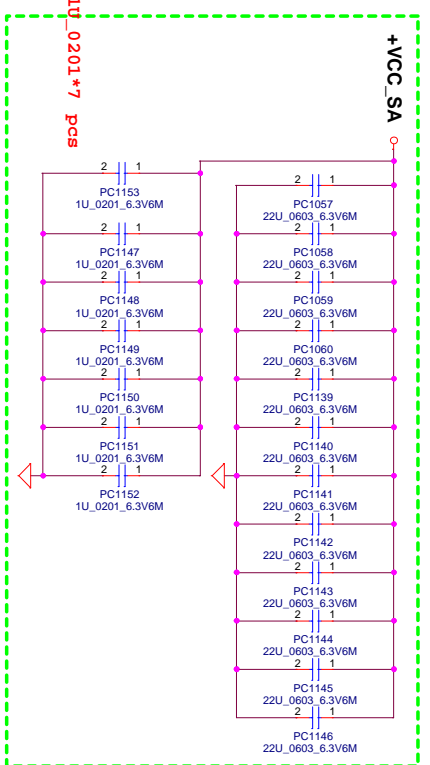
VCC GT Place on CPU (U22)  
 22U\_0603 \* 19 pcs + 1U\_0201 \* 14 pcs  
 +220u\_D7\*2 pcs



+VCC\_GT +VCC\_CORE

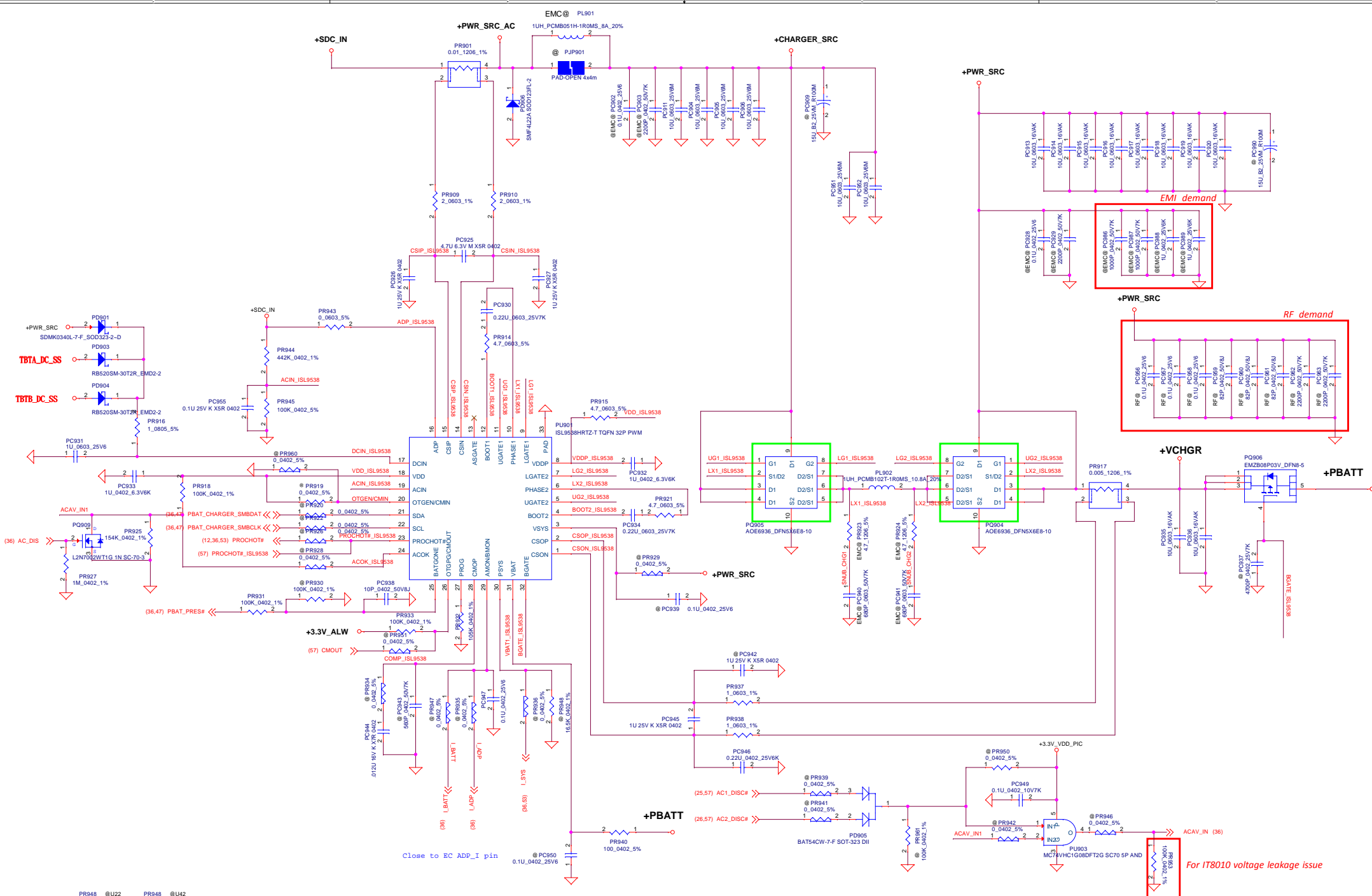
+VCC\_GT

VCC SA Place on CPU  
 22U\_0603 \* 12 pcs + 1U\_0201\*7 pcs




VCC GT +VCC\_CORE Place on CPU  
 22U\_0603 \* 6 pcs + 1U\_0201 \* 5 pcs

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		PWR charger_ISL9538	
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# Version Change List ( P. I. R. List ) LA-F292P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	MEC5105	2017/05/16	EE	for smbclk/data missed on EVT CKT	UE2.P19 USH_EXPANDER_SMBCLK UE2.P20 USH_EXPANDER_SMBDAT	0.2(X01)
2	22	HDMI MEC5105	2017/05/16	EE	GPIO naming	DISPLAY_HPD_EC change to DISPLAY_HPD_EC#	0.2(X01)
3	37	Power control MEC5105	2017/05/16	EE	CKT naming error	UE1.H5 HW_GPS_DISABLE# naming to GPS_DISABLE#	0.2(X01)
4	37	Power control MEC5105	2017/05/16	EE	modify WLAN PWR enable control CKT	Add QZ15 ,RZ517,RZ518 EC GPIO133 change to "SLP_WLAN#_GATE"	0.2(X01)
5	36	AR	2017/05/23	EE	for AR	Add RE506 Contact "TBT_RESET_N_EC" From UE2 to UT1	0.2(X01)
6	25	PD	2017/05/23	EE	BOM error	change RT87,RT88 to stuff change RT89,RT90 to non-stuff	0.2(X01)
7	43	screw hole	2017/05/16	EE	part reference naming error	"ST1 " change to "ST1", delete unnecessary space	0.2(X01)
8	57	Type C	2017/05/24	EE	AR layout	Change RT159 pop	0.2(X01)
9	52	Type C	2017/05/24	EE	AR layout	add RT409,RT410 UT1.J4 from TBTA_I2C_INT Change to TBTB_I2C_INT_R & Add0 ohm to TBTB_I2C_INT UT1.E2 from TBTB_I2C_INT Change to TBTA_I2C_INT_R & Add0 ohm to TBTA_I2C_INT swap PA to TBTB, PB to TBTA	0.2(X01)
10	56	Type C	2017/05/24	EE	AR layout	Change ROM From TBTA to TBTB Del FLASH Conn. Change RT63 to @ RT218 change to TBTA_ROM_CLK_PD Pull-Down RT219 change to TBTA_ROM_DI_PD Pull-Down RT220 change to TBTA_ROM_DO_PD Pull-Down RT221 change to TBTA_ROM_CS#_PD Pull-Up to +3.3V_TBTA_FLASH	0.2(X01) 0.2(X01)
11	36	PD	2017/05/25	EE	EC to PD SMB swap	see 0525 swap list follow EC request SMB ADDR need same with NAR SKU, SWAP UPD1/UPD2 SMB	0.2(X01)
12	36	EC MEC5105	2017/05/25	EE	EC control power phase EC SWAP	see 0525 swap list follow EC request need to swap 1.DCIN1_EN and DCIN2_EN 2.VBUS1_ECOK and VBUS2_ECOK	0.2(X01)
13	36	EC MEC5105	2017/06/01	EE	DFB request	YE1 change PN from SJ10000PW00 to SJ10000Q400	0.2(X01)
14	36	EC MEC5105	2017/06/01	EE	BOM error	Change RE95 to stuff	0.2(X01)
15	22	HDMI	2017/06/01	EE	HDMI EA test	change CT203 to @ change RV32 to 200_0402_1% SD034200080	0.2(X01)
16	28	BOARD_ID	2017/06/01	EE	BOARD_ID	RE79 Change to 130k ohm	0.3(X02)
17	35	codec	2017/06/01	EE	DFB request	LA13 footprint change to TAI-T_HCB2012KF-121T50_2P DFX requirement	0.3(X02)
18	32	Card Reader	2017/06/02	EE	GPIO	RTK Vic suggest add GPIO1 PU UR1.32 from SD_GPIO change to SD_GPIO0 UR1.1 PU 10K to +3.3V MMI_IN	0.3(X02)
19	36	EC MEC5105	2017/06/02	EE	modify WLAN PWR enable control CKT	1.UE1.D9 from SLP_WLAN#_GATE Change to SIO_SLP_WLAN# 2.NGFF_CONFIG_1 PU RE552 Cheange Location to RE562 3.SLP_WLAN#_GATE contact to EC GPIO114(Add RE552)	0.3(X02)
20	36	EC MEC5106	2017/06/02	EE	align schematic	1. RE563 change Location to RE600 2. RE564 change Location to RE601 3. RE565 change Location to RE602 4. RE566 change Location to RE603	0.3(X02)

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Item	Page#	Date	Issue Description	Solution Description	Rev.
1	57	2017/06/6	TI symbol shortage issue	PQ904 / PQ905 change to AOE6936 (SB00001JP00) because TI shortage issue	X01
2	55	2017/06/6	TI symbol shortage issue	PU610 / PU612 / PU613 change to FDMF3035 (SA0000AHX00) because TI shortage issue	X01
3	57	2017/06/14	NA	Change PR915,PR909,PR910,PR937,PR938 size from 0402 to 0603 because Charger IC version update fine-tune	X01
4	52	2017/06/14	NA	JUMP PJP403 / PJP404 change to PL407 / PL408 EMI bead	X01
5	55	2017/06/14	NA	Add un-stuff footprint PC693 ~ PC696 for RF request	X01
6	57	2017/06/14	NA	Add un-stuff footprint PC990 B2 size footprint for acoustic concern	X01
7	57	2017/06/14	NA	Add PL901 EMI choke for EMI request	X01
8	49	2017/06/14	For thermal derating concern	Change +5V_ALW output MLCC type from X5R to X6S for more thermal derating	X01
9	58	2017/06/14	Vendor sample EOL	Change MOS solution to 2nd source from AON7409 to EMZB08P03V because vendor EOL Location : PQ1202,PQ1203,PQ1211,PQ1212,PQ906	X01
10	54	2017/06/14	Vendor sample EOL	Change MOS solution to 2nd source from AON7934 to PE642DT because vendor EOL Location : PQ614	X01
11	55	2017/08/4	For new CPU driver MOS fine-tune R/C value	For nAR U22 1. PR636 from 665 change to 732 2. PR651 from 113K change to 105K 3. PR613,PR629 from 86.6K change to 88.7K 4. PC626,PC646 from 0.01uF change to 0.047uF 5. PC624,PC642 from 0.033uF change to 0.022uF	X02
12	55	2017/08/4	For new CPU driver MOS fine-tune R/C value	For nAR U42 1. PR636 from 665 change to 732 2. PR651 from 113K change to 105K 3. PR629 from 86.6K change to 88.7K 4. PC626 from 0.033uF change to 0.1uF 5. PC646 from 0.01uF change to 0.047uF 6. PC624,PC642 from 0.033uF change to 0.022uF	X02
13	55	2017/08/4	For new CPU driver MOS fine-tune R/C value	For AR U42 1. PR636 from 665 change to 732 2. PC626 from 0.033uF change to 0.1uF 3. PC624 from 0.033uF change to 0.01uF 4. PC646 from 0.01uF change to 0.047uF 5. PC642 from 0.033uF change to 0.022uF	X02
14	55	2017/08/10	Stuff component for RF request	1. PR202 and PC204 change to stuff 2. PR663 and PC662 change to stuff 3. PC693, PC694, PC695 change to stuff	X02
15	57	2017/08/10	Reserve footprint for chagrer input	Add PD906 for footprint reserve	X02
16	57		Reserve footprint change to stuff	PD906 reserve footprint change to stuff	A00

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**PWR P.I.R**

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
21	36	MEC5105	2017/06/07	EE	UPD1_HPD/UPD2_HPD	RE553/RE554 resistor to 1M ohm(change to SD028100480)	0.3(X02)
22	11	CPU(6/14)	2017/06/15	EE	Microchip request	RC444 Change to @	0.3(X02)
23	39	USH	2017/06/15	EE	NPCT75x	Pop RZ89, RZ365, RZ112,Depop RZ367, RZ366, RZ62, RZ363	0.3(X02)
24	11	CPU(6/14)	2017/06/15	EE	SUSACK#	SUSACK#_R Reserved RC550 PU 1K to +3.3V_1.8V_PGPPA	0.3(X02)
25	11	CPU(6/14)	2017/06/15	EE	XTAL	RC417,RC418 change to 33 ohm	0.3(X02)
26	38	TPM	2017/06/15	EE	NPCT750	RZ69.1 From +UZ12_VHIO Change to +3.3V_ALW_PCH	0.3(X02)
27	12	CPU(7/14)	2017/06/15	EE	ME Lock	RC223.1 from ME_FWP change to ME_FWP_SW	0.3(X02)
28	9	CPU	2017/07/27	EE	align schematic	Reserved RC557 PU,RC558 PD	0.5(X04)
29	23	AR	2017/07/27	EE	align schematic	Add RT419 RT420 & Add RT421 to EC& Reserved RT422 to PCH	0.5(X04)
30	9	CPU	2017/07/27	EE	align schematic	Remove RC405	0.5(X04)
31	22	HDMI	2017/08/07	EE	EMI request	LV31~LV36 Change to 8.2 ohm & LV37~LV38 Change to 15nH, CT201 <CT202 CT20 4 chang e t o @	0.5(X04)
32	37	EC	2017/08/08	EE	BOARD ID	BOARD ID RE79 From 130K change to 62K	0.5(X04)
33	9	CPU (4/14)	2017/08/09	EE	RTD3	Reserved RC559	0.5(X04)
34	9	CPU (4/14)	2017/08/09	EE	RTD4	Add RC560 Reserved RC561	0.5(X04)
35	25 、 26	PD	2017/08/09	EE	PD	PJP7 Change to RT450 Reserved Add RT451 to +3.3V_ALW PJP9 Change to RT452 Reserved RT453 to +3.3V_ALW	0.5(X04)
36	23	AR	2017/08/10	EE	RTD3	Add RT456 For RDT3	0.5(X04)
37	9	CPU (4/14)	2017/10/30	EE	GPIO map change	Depop RC330, RC331	1.0(A00)
38	12	CPU (7/14)	2017/10/30	EE	ME SW depop	Depop RC222, SW1, RC221 change to 0 ohm short pad	1.0(A00)
39	44	PAD,LED	2017/10/30	EE	PWR SW depop	Depop SW3	1.0(A00)
40	38	MEC5105 support	2017/10/30	EE	UE2 depop	Depop UE2,CE501,CE502,RE501,RE503,RE528,RE504,CE500	1.0(A00)
41	38	MEC5105 support	2017/10/30	EE	BOARD ID	BOARD ID RE79 From 62K change to 4.3K	1.0(A00)
42	8	CPU (3/14)	2017/10/30	EE	Add solder mask	Add footprint -NPM on UC6	1.0(A00)
43	23 、 34	HDMI CONN & NGFF Card	2017/10/30	EE	DFX request	Add footprint -NPM on LV3, LV6, LV9, LV12, RI27, RI28, RI29, RI30, RI47, RI48, RI49, RI50	1.0(A00)
44	39	USH & TPM	2017/10/30	EE	TPM A-rev.	UZ12 SA0000AQ200->SA0000AQ220	1.0(A00)
45	All	All	2017/10/30	EE	0 ohm change to short pad	0 ohm change to short pad	1.0(A00)
46	27	[Type C] PD Power-2	2017/10/30	EE	Change Part Number	UT7 SA00009TZ00 change to SA00009TZ10	1.0(A00)
47	25 、 26	[Type C] PD Controller	2017/10/30	EE	PD change main source	UT5 UT11 SA0000AX700 change to SA0000BIJ00	1.0(A00)

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48	9, 23	TBT-AR-DP (1/2) DP, PCIE	2017/10/30	EE	RTD3_CIO_PWR_EN PU change	Depop RT372,    pop RC559	1.0(A00)
49	23	TBT-AR-DP (1/2) DP, PCIE	2017/10/30	EE	EMI HDMI request	CT201,CT202 depop	1.0(A00)
50	22	HDMI CONN	2017/10/30	EE	EMI HDMI request	RV32    SD034200080->SD028360080 LV31,LV32,LV33,LV34,LV35,LV36    SHI0000JI00->SHI0000I300	1.0(A00)
51	25 、 26	[Type C] PD Controller	2017/11/02	EE	Material change	CT74,CT83,CT150    SE000010V00->SE00000QL10	1.0(A00)

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